Design Approaches for Low-Power Reconfigurable Analog-to-Digital Converters

A Thesis

Presented in Partial Fulfillment of the Requirements for

the Degree Master of Science in the

Graduate School of The Ohio State University

By

Omer Can Akgun, B.S

* * * * *

The Ohio State University

2004

Master's Examination Committee:

Prof. Mohammed Ismail, Adviser

Prof. Steven Bibyk

Approved by

Adviser

Department of Electrical Engineering

ABSTRACT

With the recent advancements in integrated circuit technology, digital CMOS circuits have been exponentially scaled according to Moore's Law over the last three decades. Because analog circuits cannot be scaled down as easy as the digital circuits, it's desirable to minimize analog signal processing in any integrated system. Also with developments in digital signal processing algorithms and development tools, digital signal processing has been the preferred choice of signal processing in terms of development costs and ease of implementation. To move the signal processing from the analog domain to digital domain, analog-to-digital converters are required.

To achieve lower manufacturing costs, it is desirable to have systems that can realize multiple functions or that can support multiple standards on a single chip. These kinds of systems save expensive die area and also save board space which are two qualities that are highly desired in terms of cost. For multi-function or multi-standard applications, pipelined ADCs can be used and they can be easily reconfigured in terms of resolution. However it is not easy to reconfigure pipelined ADCs for power-scaled operation.

Objective of this thesis is to investigate design approaches for reconfigurable ADCs with the linear power-speed scaling feature. Reconfigurable low-power ADC designs are useful in mixed-signal systems where the power consumption is an issue, like multi-standard wireless handsets and portable digital video applications.

The reconfigurable architecture proposed in this thesis achieves the desired feature of scaling power linearly with speed. The basic pipelined ADC is reconfigured as a cascade of cyclic ADC stages to achieve power-speed scaling. A novel Capacitor Reuse Technique is also proposed to minimize the amount of additional hardware to realize the reconfigurable operation.

Design Approaches for Low-Power Reconfigurable Analog-to-Digital Converters

By

Omer Can Akgun, M.S.

The Ohio State University, 2004

Prof. Mohammed Ismail, Adviser

With the recent advancements in integrated circuit technology, digital CMOS circuits have been exponentially scaled according to Moore's Law over the last three decades. Because analog circuits cannot be scaled down as easy as the digital circuits, it's desirable to minimize analog signal processing in any integrated system. Also with developments in digital signal processing algorithms and development tools, digital signal processing has been the preferred choice of signal processing in terms of development costs and ease of implementation. To move the signal processing from the analog domain to digital domain, analog-to-digital converters are required.

To achieve lower manufacturing costs, it is desirable to have systems that can realize multiple functions or that can support multiple standards on a single chip. These kinds of systems save expensive die area and also save board space which are two qualities that are highly desired in terms of cost. For multi-function or multi-standard applications, pipelined ADCs can be used and they can be easily

reconfigured in terms of resolution. However it is not easy to reconfigure pipelined ADCs for power-scaled operation.

Objective of this thesis is to investigate design approaches for reconfigurable ADCs with the linear power-speed scaling feature. Reconfigurable low-power ADC designs are useful in mixed-signal systems where the power consumption is an issue, like multi-standard wireless handsets and portable digital video applications.

The reconfigurable architecture proposed in this thesis achieves the desired feature of scaling power linearly with speed. The basic pipelined ADC is reconfigured as a cascade of cyclic ADC stages to achieve power-speed scaling. A novel Capacitor Reuse Technique is also proposed to minimize the amount of additional hardware to realize the reconfigurable operation.

This work is dedicated to my family.

ACKNOWLEDGMENTS

I would like to express my sincere gratitude to my advisor Prof. Mohammed Ismail for providing the guidance and resources that were vital to successful completion of my Masters' program.

I would also like to thank Prof. Steven Bibyk for being a part of my Master's examination committee and for his very useful comments about the oral examination presentation.

I would also like to thank Scandinavian metal bands for keeping me awake for many long nights during the course of my studies, Raistlin for showing the real meaning of being ambitious, and Cartman from South Park for being my idol.

Most of all, I am very grateful to my family, who have always supported me through out the course of my life both emotionally and financially, and provided me every opportunity to successfully conclude my studies.

Lastly, I would like acknowledge the support of my colleagues at The Ohio State University, namely Anup Savla, Golsa Ghiaasi Hafezi, Arun Ravindran, Jennifer Leonard and others, who have broadened my horizons with many technical discussions, and helped me survive the politics of the 'land'.

VITA

June 18, 1980	Born - Istanbul, Turkey
June 2002	B.Sc. Electronics and Telecommunication Engineering, Istanbul Technical University, Istanbul, Turkey
September 2002-Present	Graduate Student, The Ohio State University.

PUBLICATIONS

Research Publications

Omer Can Akgun, Anup Savla, Mohammed Ismail

"A Reconfigurable Pipelined ADC with Linear Power-Speed Scaling", *Journal of Analog Integrated Circuits and Signal Processing*, submitted for review.

FIELDS OF STUDY

Major Field: Electrical Engineering

Studies in:

Studies in Solid State Circuits - Analog VLSI Lab.: Prof. Mohammed Ismail

TABLE OF CONTENTS

Page

LIST OF TABLES

LIST OF FIGURES

Figure **Page**

CHAPTER 1

INTRODUCTION

Data converters are paramount in modern data and voice communication systems, digital imaging devices and magnetic storage devices where increasing complexity of signal processing is mostly done in the digital domain. With the developments in the digital signal processing development tools and algorithms and increasing density of the digital circuitry in the integrated circuits, the digital signal processing has been the choice of signal processing domain. However, because all natural signals are analog, analog-to-digital converters (ADCs) are needed to transfer the information to be processed from the analog domain to the digital domain.

1.1 Motivation and Research Goals

Analog-to-digital converters (ADCs) capable of scaling power consumption with changing resolution and speed requirements are desirable in many applications. For example, multi-standard receivers operating with different sensitivity levels and channel bandwidths place varying requirements on the ADC [1]. Another example is portable electronic devices such as hand-held video and photo cameras, which require ADCs to function with different speeds and resolution based on the quality of the image processing required [2].

Wireless Standard	Channel Bandwidth (MHz)
WLAN 802.11a	20
WLAN 802.11b (DSSS)	22
WLAN 802.11b (FHSS)	1
Bluetooth	1
WCDMA	3.84

Table 1.1: Channel Bandwidths for various communication standards

In multi-standard mobile communication systems, ADCs are required to operate at a wide range of conversion speeds with low-power consumption [13]. In recent years, pipelined switched-capacitor ADCs have been used for low-power, high-speed applications with medium to high resolution. The pipeline architecture has distinct power and area advantages over the flash topology, and can sample at higher clock speeds than successive approximation or cyclic topologies. Also with over-sampling sigma-delta ADCs the required ADC bandwidth cannot be achieved [3].

Table 1.1 shows the channel bandwidths for different wireless communication standards. For a direct conversion receiver, depending on sensitivity and anti-aliasing requirements, the required ADC sampling rate can vary between 1MS/s and 22MS/s for multi-mode operation.

Reconfigurable ADC architectures attempt to combine advantages of different ADC topologies, thereby enhancing their performance in terms of speed, resolution or power consumption. Previously reported reconfigurable ADCs include a sigma-delta pipeline hybrid ADC [5], a dual mode flash ADC [6], and a reconfigurable cyclic ADC that can operate with three different resolutions [7].

In a pipelined ADC power consumption can be easily scaled with varying resolution by operating only the required number of stages and powering down the remaining stages. In contrast, scaling power for different speeds is not feasible because unlike digital logic, analog circuits continuously dissipate power regardless of switching rate. Since most of the power consumption in a pipelined ADC can be attributed to operational transconductance amplifiers (OTAs), the same amount of power will be dissipated at any sampling speed. In a multi-standard or multi-function design, this leads to inefficient operation at low sampling speeds.

The main goal of this thesis is to develop an ADC architecture that can linearly scale power with speed which can be used in multi-function and multi-speed applications. A practical demonstration of the feasibility of the proposed architectures is also aimed.

To verify the effectiveness of the proposed techniques and the ADC topology, a 10-bit 20MS/s reconfigurable pipelined ADC is designed in $0.5\mu m$ CMOS technology. The simulation results show that the effective number of bits (ENOB) changes from 9.97 to 9.52 for different modes of operation with better than linear power-speed scaling. Power consumption is 28.8 mW at 20MS/s conversion speed and 6.85 mW at 5MS/s.

1.2 Organization of Thesis

This thesis is divided into six chapters.

In this introduction chapter the need for ADCs and reconfiguration is explained.

Chapter 2 explains the analog-to-digital conversion concept and commonly used parameters for ADC characterization. Also various ADC architectures are presented.

Chapter 3 describes the cyclic and pipelined ADC architectures and digital correction.

Chapter 4 demonstrates the reconfigurable ADC architecture in both the system and circuit levels. Also in this chapter novel capacitor reuse technique is explained.

Chapter 5 presents the design of the main circuit blocks and simulation results for five modes of operation.

Chapter 6 contains the summary of the results and proposals for the future work.

CHAPTER 2

ANALOG TO DIGITAL CONVERTER ARCHITECTURES AND CHARACTERIZATION

2.1 Overview

With the developments in integrated circuit technology and the cost of digital signal processing decreasing, ADC architectures have been a topic of extensive research in the recent years. Numbers of different ADC architectures have been proposed in the past, each representing trade-offs between conversion speed, resolution, power consumption and die area.

In this chapter the concept of analog-to-digital conversion and commonly used parameters for ADC characterization are described. Different ADC architectures, along with their advantages and disadvantages are presented.

2.2 Ideal Analog to Digital Converter

The block diagram representation of an ADC is shown in Figure 2.1. In the diagram V_{in} is the analog input signal, V_{ref} is the reference voltage and B_{out} is the digital output word. Also, V_{LSB} is defined as the analog signal value change corresponding to a single least significant bit (LSB) change in the digital word and is given by equation 2.1 where N is the resolution of the ADC [15].

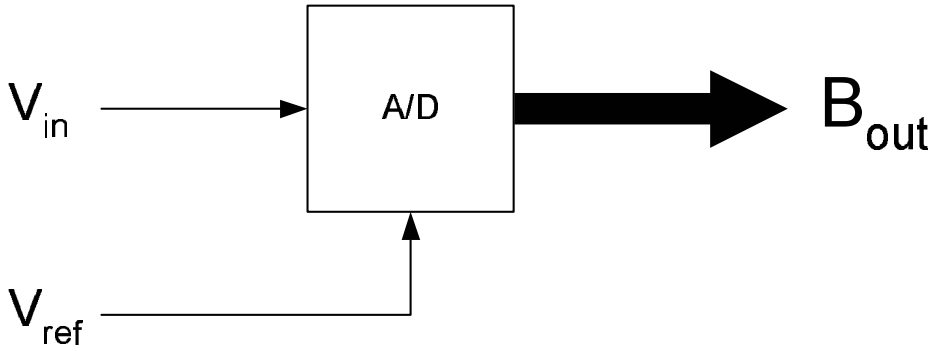


Figure 2.1: A block diagram for an A/D converter.

$$V_{LSB} = \frac{V_{ref}}{2^N} \tag{2.1}$$

The analog value of the converted digital word can be found using equation 2.2.

$$V_{out} = V_{ref}(b_1 2^{-1} + b_2 2^{-2} + b_3 2^{-3} + \ldots + b_N 2^{-N}) \tag{2.2}$$

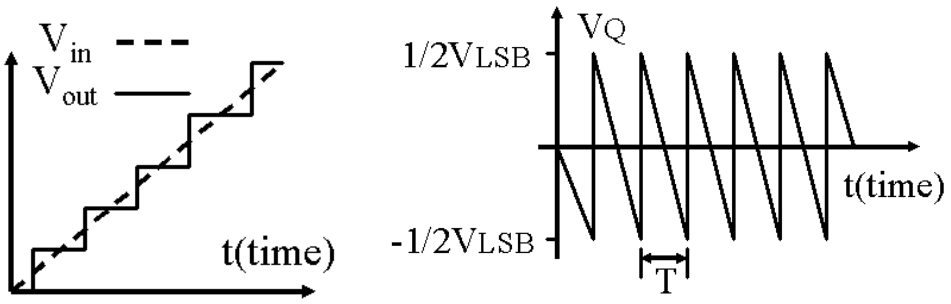
The difference between the analog value of the resolved digital word and the actual analog input is given by

$$V_{out} - V_{in} = V_x = V_Q \tag{2.3}$$

where

$$-\frac{1}{2}V_{LSB} \leq V_x \leq \frac{1}{2}V_{LSB} \tag{2.4}$$

The difference in equation 2.3 results from the fact that the resolved value is finite in precision and it is called the "quantization error". The quantization error can be



a. Input ramp b. Quantization error

Figure 2.2: Input ramp signal and respective quantization error.

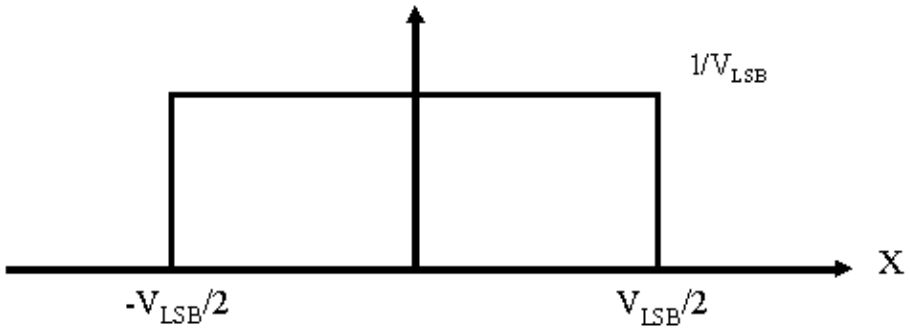


Figure 2.3: Probability density function of quantization error.

seen by applying a ramp input to the ADC input and taking the difference between the input and the resolved output (Figure 2.2).

The quantization error occurs even in ideal ADCs and the noise due to the quantization error can be calculated as follows:

It's assumed that the input signal is varying rapidly such that the quantization error signal, V_Q, is a uniform random variable within the range $[-\frac{V_{LSB}}{2}, \frac{V_{LSB}}{2}]$. The probability density function for such a signal will be constant in the defined range as shown in Figure 2.3.

The root mean square (rms) value of the quantization error is given by

$$V_{Q(rms)} = \sqrt{\int_{-\infty}^{\infty} x^2 f(x) dx} = \sqrt{\frac{1}{V_{LSB}} (\int_{-V_{LSB}/2}^{V_{LSB}/2} x^2 dx)} = \frac{V_{LSB}}{\sqrt{12}} \tag{2.5}$$

and the noise power is given by

$$\sigma^2 = \frac{V_{LSB}^2}{12} \tag{2.6}$$

2.3 ADC Characterization

ADC performance must be measured in the context of their applications. Characterization by static (DC) parameters have been used for low-speed applications such as low-speed sensors, disk drives and micro-controllers. The static parameters include offset, linearity, gain error, integral non-linearity (INL) and differential non-linearity (DNL). However, characterization for high speed applications such as digital communications, IF digitization, magnetic storage and high definition TV (HDTV) must be done using dynamic parameters.

2.3.1 Static Parameters

DC performance of the ADCs can be characterized by examining their conversion voltage thresholds. The transfer response of an ADC can be defined as the mid-points of the quantization intervals for each distinct digital output word. However, measuring the transitions are easier than measuring the mid-point values, so errors are often measured in terms of transition points. Some of the static performance parameters of the ADC are described below.

Resolution: The resolution of a converter is defined as the fineness of quantization performed by the ADC. An N-bit ADC can resolve the analog input value into $2^N - 1$ distinct digital values.

Accuracy: The accuracy of an ADC is defined to be the difference between the expected and actual transfer responses. The accuracy includes the effects of offset, gain and linearity errors, which will be described in the following paragraphs. An N-bit converter can have less than N-bit accuracy due to deterministic and random errors.

Offset Error: Offset error occurs when there is a difference between the value of the first code transition and the ideal value of 1/2 LSB. The offset error is a constant value for all the transition values.

Gain Error: Gain error is the difference in the slope of a straight line drawn through the transfer characteristic of the ADC and a straight line with a slope of 1 which represents an ideal ADC.

INL: After removing both the offset and gain errors, INL is defined to be the deviation from a straight line. Usually a best-fit transfer line is used for calculations. An ADC with N-bit resolution migth have a lower accuracy if its INL exceeds 1/2 LSB.

DNL: For an ADC, DNL is the difference between the actual code width of nonideal converter and an ideal converter. In an ideal ADC the transition values are precisely 1 LSB apart. The values for the DNL can be found as follows:

$$DNL = Actualstepwidth - Idealstepwidth \tag{2.7}$$

DNL of more than 1 LSB can mean there exists an analog voltage sub-range which cannot be resolved into any digital value, and this results in missing codes.

2.3.2 Dynamic Parameters

Dynamic performance parameters of an ADC depend on the resolution, the sampling and input frequencies and include information about the linearity, distortion, sampling time uncertainty, noise and settling errors [22].

Performing a Fast Fourier Transform (FFT) of the output is usually used for characterizing an ADC dynamically. A sample plot is shown in Figure 2.4. The shown spectrum contains the input sine wave, quantization error and harmonic distortion caused by nonlinearity. The input frequency should be chosen carefully so that the harmonics do not add to the fundamental signal. Also appropriate windowing function should be applied to the FFT data to minimize spectral leakage [23].

Signal-to-Noise Ratio: The Signal-to-Noise Ratio (SNR) is the ratio of the signal power to the noise power at the converter output. The SNR includes the quantization and the circuit noise but it does not include the harmonic noise or noise due to circuit nonlinearities . The maximum achievable SNR is given by

$$SNR_{max} = 6.02N + 1.76(dB) \tag{2.8}$$

Total Harmonic Distortion: The Total Harmonic Distortion (THD) can be expressed as

$$THD = \frac{\sqrt{\sum_{n=2}^{N_H+1} A^2(nf_{in})}}{A(f_{in})} \tag{2.9}$$

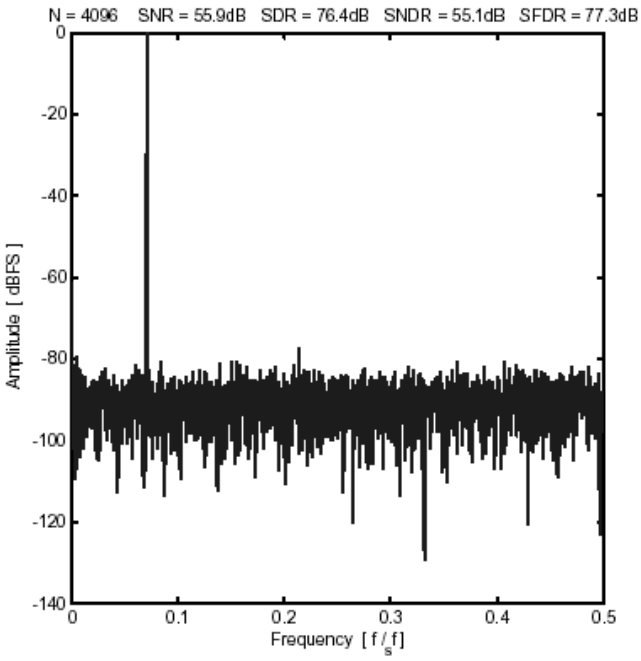


Figure 2.4: FFT of an ADC output.

where N_H, $A(f_{in})$ and $A(nf_{in})$ are the number of harmonics taken into consideration, the amplitude of the output signal at the input frequency and the amplitude of the nth harmonic at the output, respectively.

Spurious Free Dynamic Range: Spurious Free Dynamic Range (SFDR) is defined as the ratio between the maximum amplitude of the signal component and the amplitude of the largest distortion component. SFDR is an indicator showing the spectral purity of the ADC.

Signal-to-Noise plus Distortion Ratio: The Signal-to-Noise plus Distortion Ratio (SNDR) is the ratio between the amplitude of the main signal component and the noise plus the distortion power measured at the ADC output.

Effective Number of Bits: The Effective Number of Bits (ENOB) summarizes the dynamic performance of the ADC and can be defined for different input frequencies. The ENOB is given by

$$ENOB(f_{in}) = \frac{SNDR_{db}(f_{in}) - 1.76}{6.02} \tag{2.10}$$

and is a direct indicator of the the accuracy of the ADC.

2.4 ADC Architectures

2.4.1 Flash

The Flash ADCs can reach very high conversion speeds since their only analog building block is the comparator. The flash ADC topology is shown in Figure 2.5. The reference levels are usually generated by an on-chip resistor string. The signal at the output of the comparators is thermometer coded representation of the input signal and a $2^N - 1$ to N encoder is needed at the comparator outputs to convert the thermometer code to binary code.

The main problem with the flash architecture is that the number of comparators increase exponentially with resolution and the total number of comparators is $2^N - 1$, where N is the resolution of the ADC. Another problem due to the large number of comparators is the input capacitance of the ADC. Because of this high input capacitance, the circuit driving the ADC must consume a high amount of power.

2.4.2 Two-step

To reduce the number of comparators in a flash ADC, the two-step architecture was developed. In this type of ADC a coarse ADC generates the most significant

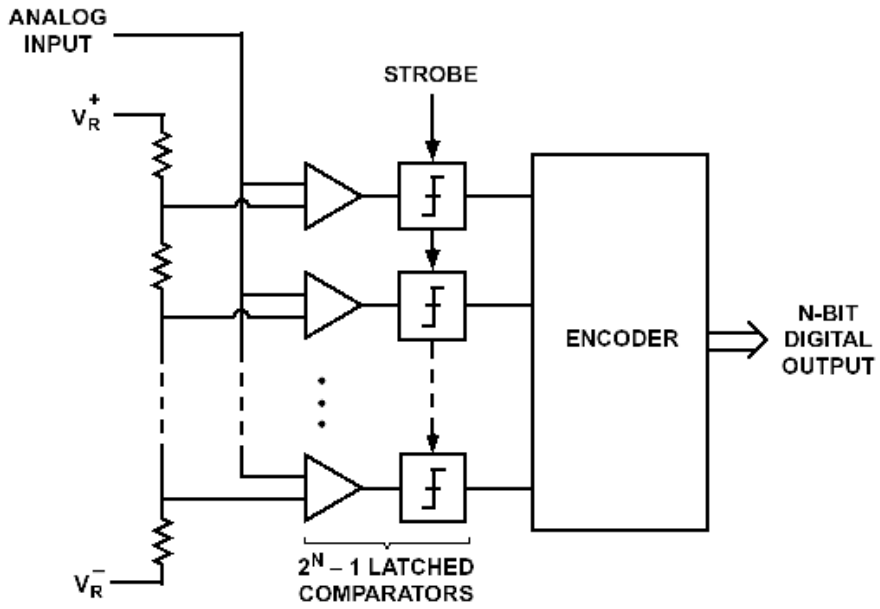


Figure 2.5: The Flash ADC.

bits. These generated bits are converted to an analog value using a digital-to-analog converter (DAC) and by subtracting this value from the input value the residue is generated. From the newly generated residue fine bits are generated using a second ADC. The two-step architecture can be seen in Figure 2.6.

In the two-step topology the number of comparators needed is given by

$$2^N + 2^M - 2 \tag{2.11}$$

where N is the number of bits in the coarse ADC and M is the number of bits resolved by the fine ADC.

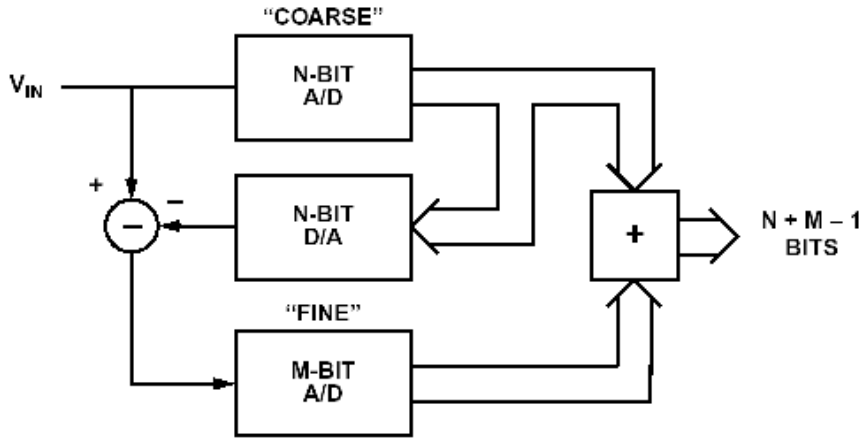


Figure 2.6: The Two-Step Flash ADC.

2.4.3 Successive Approximation Register

The Successive Approximation Register (SAR) ADC is a low-speed converter. The SAR architecture is shown in Figure 2.7 and it consists of a comparator, a DAC and a SAR. Starting with the MSB the comparator determines if the input signal is greater or less than the DAC output. The resulting bits are stored in the SAR and are used for generating the new comparison level. This process is repeated for N times for an N bit SAR ADC, therefore the speed is greatly reduced when the required resolution is high.

2.4.4 Sigma-delta

The Sigma-Delta ADCs are based on the fact that the quantization error can be high-pass filtered and later removed by digital filters. The requirements on the analog parts are relaxed and higher resolutions can be achieved [24],[25]. The drawback of this type of converter is that for high resolutions the signal bandwidth must be kept

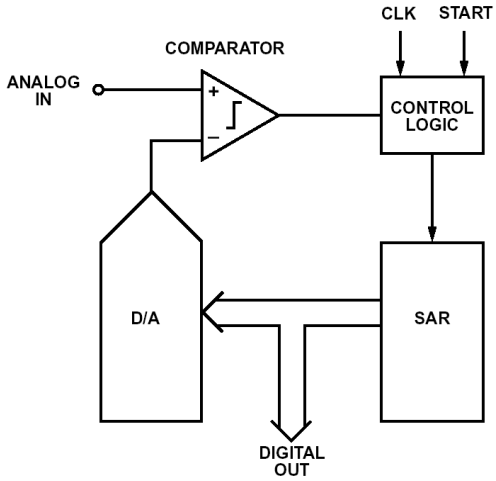


Figure 2.7: The Successive Approximation Register ADC.

small, thus limiting the applications of this kind of architecture. A 1-bit Sigma-Delta modulator is shown in Figure 2.8.

2.4.5 Integrating

The integrating ADCs are generally used for realizing high-accuracy conversion of very slow-moving signals. These type of ADCs have very low offset and gain error, and they are highly linear. Another advantage of integrating ADCs is the small amount of circuitry required. A single slope integrating converter is shown in Figure 2.9.

In the integrating converters input is converted to a timing pulse, and the width of this pulse is measured by counting clock cycles. The number of clock cycles required for converting the signal to N bits is 2^N. Integrating ADCs are usually used in the low-frequency instrumentation applications due to their slow conversion speed.

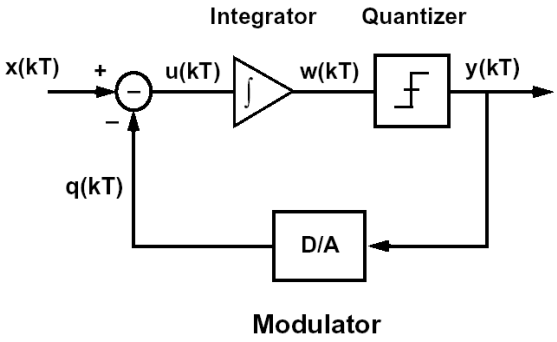


Figure 2.8: 1-bit Sigma-Delta modulator.

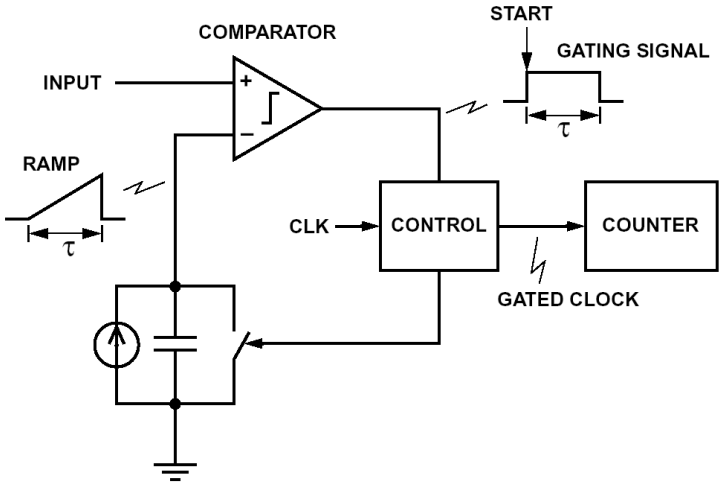


Figure 2.9: A Single Slope Integrating Converter

CHAPTER 3

PIPELINED AND CYCLIC ADC ARCHITECTURES

3.1 Overview

In this chapter the pipelined and cyclic ADC architectures are presented. The evolution of the pipelined ADC concept and the main blocks in the pipelined stages are explained. The digital correction is presented and the switched capacitor implementation of pipelined stages is shown.

3.2 Cyclic ADC

A cyclic converter operates like a SAR converter by using the resolved value for conversion. However, where a SAR converter halves the reference voltage, a cyclic converter doubles the residue voltage while the reference voltage is kept constant [17], [15]. A block diagram of a cyclic ADC is shown in Figure 3.1.

The clock signals required for the operation of the cyclic ADC are shown in Figure 3.2. The input signal is sampled when the sampling clock goes high. When the amplification clock is high, the signal is compared to the reference voltage and the resolved bit is written into the shift register.

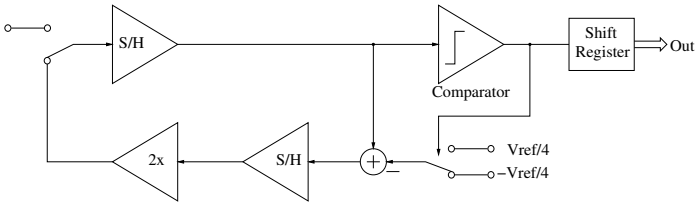


Figure 3.1: Cyclic ADC architecture.

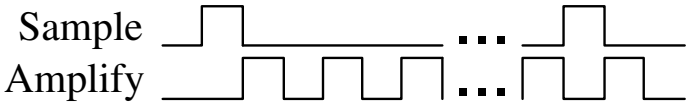


Figure 3.2: Clock signals for cyclic operation.

The sample and hold (S/H) and gain by two functions can be realized using the simple noninverting amplifier circuit shown in Figure 3.3. Here the clocks ϕ_1 and ϕ_2 are sampling and amplification clocks, respectively. During the sampling phase a charge equal to $C_1 V_{in}$ is stored on the capacitor C_1. As the sampling clock goes low, a constant charge Δq is injected into node X. As the amplification clock goes high, node P goes from V_{in} to 0. This change at node P results in the output voltage changing from 0 to $V_{in}\frac{C_1}{C_2}$, providing a voltage gain of $\frac{C_1}{C_2}$. The full circuit implementation of a cyclic ADC is shown in Figure 3.4.

Although the implementation of the cyclic ADC is simple and power consumption is low when compared to the flash or two-step ADCs, like the SAR ADC each conversion requires N clock cycles for N bit resolution, which limits the maximum conversion speed achievable.

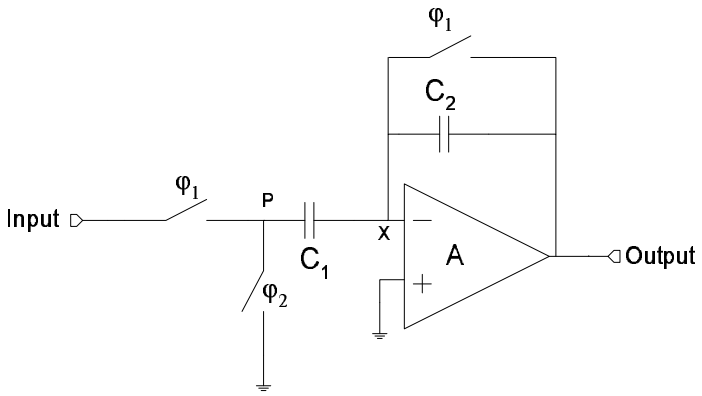


Figure 3.3: S/H and gain-by-2 circuits.

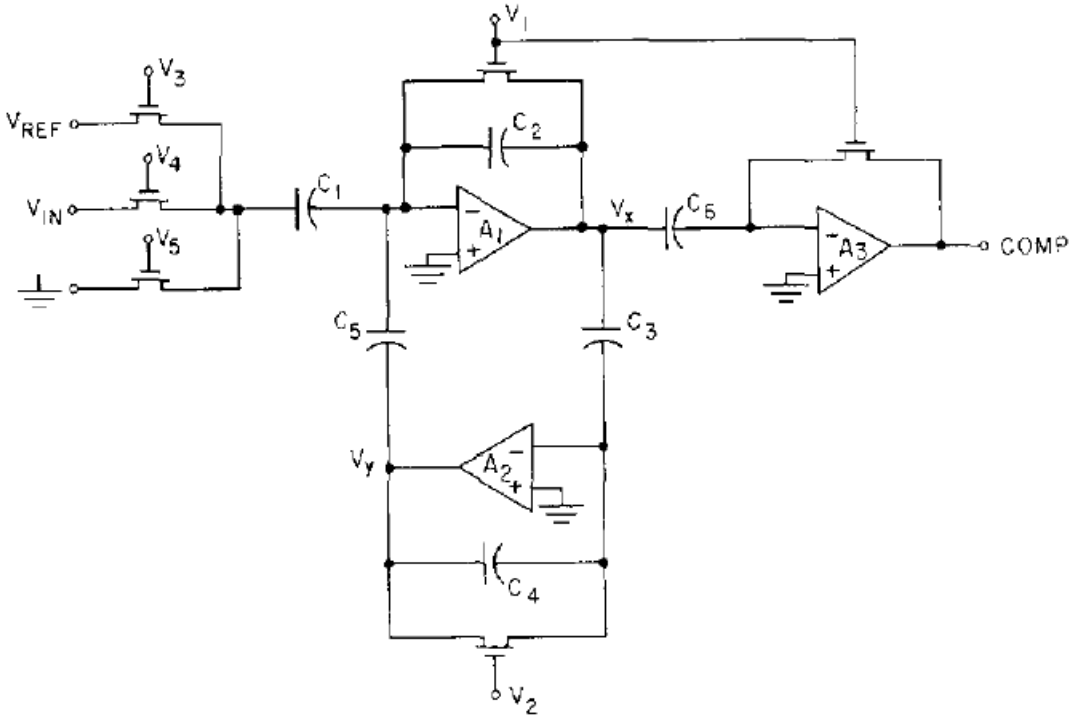


Figure 3.4: Circuit Implementation of Cyclic ADC [17].

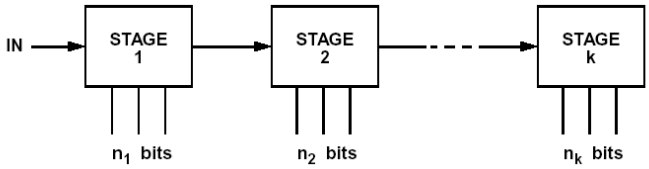


Figure 3.5: Pipelined ADC block diagram.

3.3 Pipelined ADC

The pipelined ADC can be thought as a multi-step ADC. The basic concept is the same as the two-step ADC as described in Section 2.4.2. Whereas a two-step ADC consists of 2 stages, a pipelined ADC consists of multiple stages. If every stage resolves 1-bit, for N bit conversion an N bit pipelined ADC is required.

A general pipelined ADC block diagram is shown in Figure 3.5. In general the number of bits resolved by each stage can be different. After each stage resolves its number of allocated bits, the error signal is generated, multiplied and passed onto the next stage. The following stage samples this input value, converts the digital bits, generates the residue and passes it to the next stage. This operation is repeated by all the stages of the pipeline and continues until all the bits are resolved.

A stage of a pipelined ADC which can resolve n_i bits is shown in Figure 3.6. Here the input signal is sampled by the S/H circuit and this sampled value is resolved into n_i bits by the Sub-ADC. From these resolved bits, an analog value is generated using a Sub-DAC and this value is subtracted from the sampled input signal to generate the error signal. This newly generated error signal is then multiplied by 2^{n_i} to generate the input signal to the next stage. The pipelined operation described is shown in Figure 3.7.

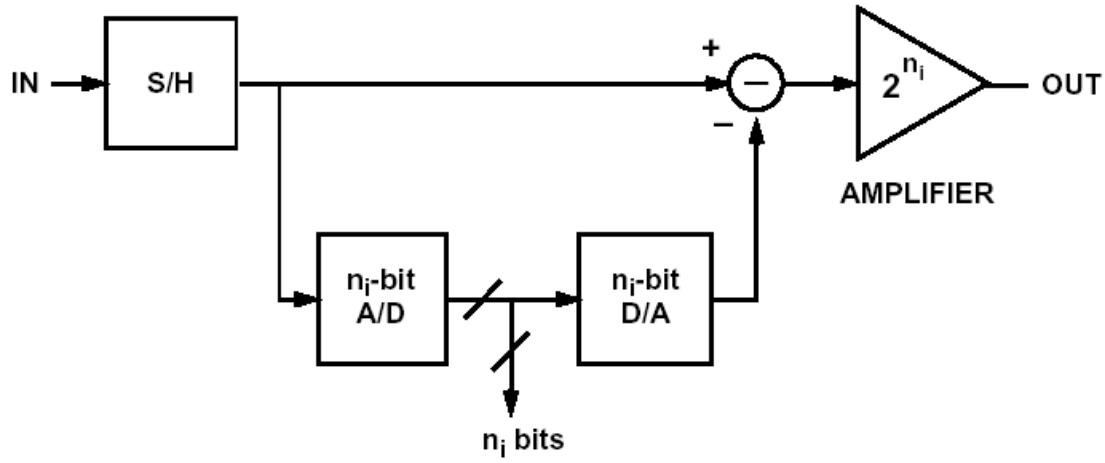


Figure 3.6: Pipelined ADC Stage Block Diagram.

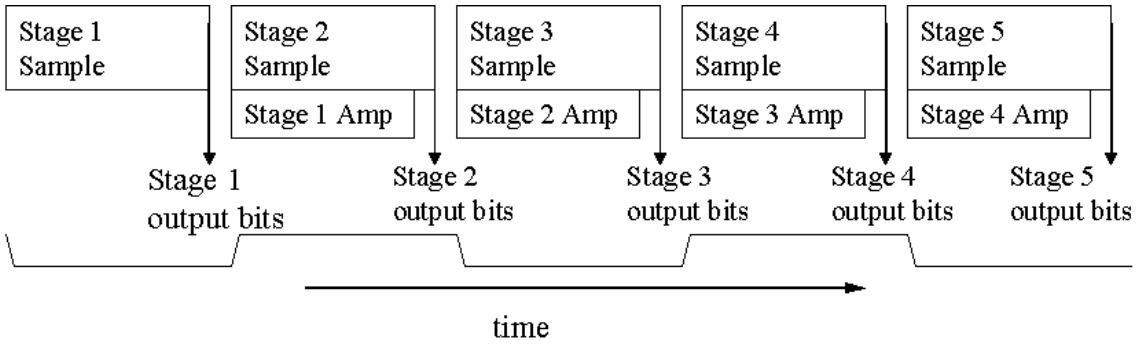


Figure 3.7: Pipelined operation timing diagram.

For the correct pipelined operation, mth stage is required to be $N - m - 1$ bits accurate, where N is the resolution of the ADC and m is the stage number. The factors limiting the stage accuracy are the gain error, finite bandwidth and slew rate limitation of the amplifier, thermal noise and comparator offset errors. Comparator offset errors can be corrected using the digital correction and will be explained in Section 3.4.

The main advantages of the pipelined ADC are the high-throughput and robust design if all the stages are the same. After an initial delay of N clock cycles (assuming 1-bit/stage conversion), one conversion will be completed per clock cycle. While the signal generated by the first stage is worked on in the second stage, the first stage can work on the next sample. The disadvantage of the pipelined ADC is having the initial N clock delay before the first output is generated. This initial delay is not important for most of the applications and it can be tolerated.

3.3.1 Sub-ADC Design

The sub-ADC used in the pipeline stages is designed as a flash ADC. For a 1-bit/stage pipelined ADC, there is only 1 comparator used in each sub-ADC. Increasing the number of bits per stage will increase the number of comparators in each stage exponentially. The comparators used in the first few stages need to be highly accurate, and for implementations of 10 bits or higher, the requirement becomes stringent. However digital correction algorithms has been developed which will be explained in Section 3.4.

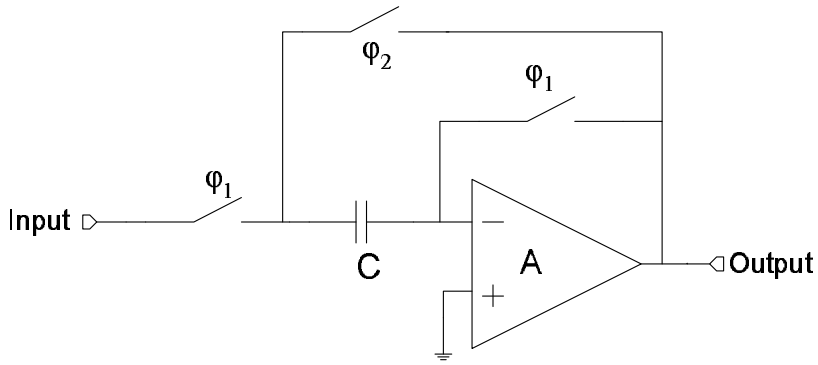


Figure 3.8: Front-end S/H circuit.

3.3.2 S/H, Sub-DAC and Residue Amplifier Design

In medium-to-high speed ADCs, the signal at the input of the ADC changes too rapidly to be applied directly to the comparators for conversion. Because of this rapid change, errors occur in the conversion process. Thus, a front-end S/H circuit is required, which makes the ADC a sampled data system. A S/H circuit is shown in Figure 3.8. In the figure, during ϕ_1 the input signal is sampled on the capacitor and during ϕ_2 the sampled signal is buffered (hold) at the amplifier output.

The Sub-DAC and the residue amplifier can be combined into a single structure which is shown in Figure 3.9. The gain of this circuit is 2 if $C_s = C_f$. The output voltage value depends on the resolved bit B and is given by

$$V_{out} = \frac{C_s + C_f}{C_s} V_{in} \pm \frac{C_s}{C_f} \frac{V_{ref}}{2} \tag{3.1}$$

which translates into

$$V_{out} = \begin{array}{ll} 2V_{in} + V_{ref}/2, & V_{in} < 0 \\ 2V_{in} - V_{ref}/2, & V_{in} > 0 \end{array} \tag{3.2}$$

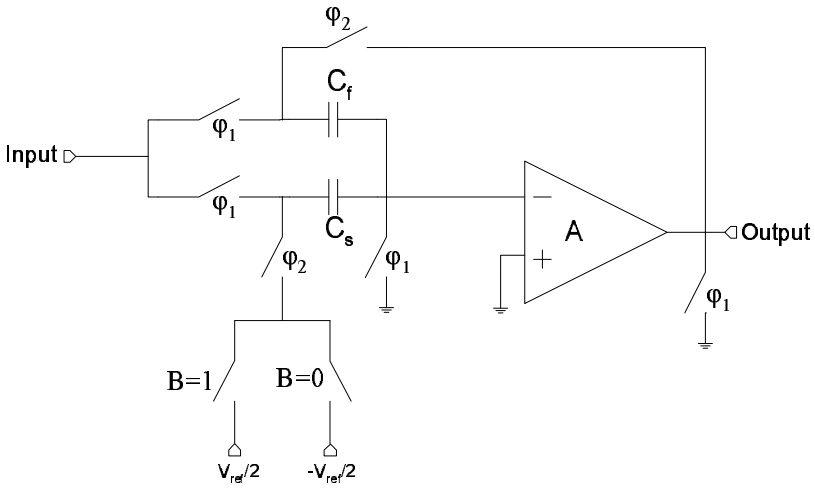


Figure 3.9: Sub-DAC and Residue Amplifier.

Also it should be noted that, after the first stage a dedicated S/H circuit is not required down the pipeline because the residue amplifier of the preceding stage is also used as a S/H amplifier, effectively holding the input signal for the next stage.

3.4 Comparator Offset Error and Digital Correction

Comparators are the fundamental building blocks of the analog-to-digital conversion operation. Due to the nature of the pipelined operation, the comparators in the first few stages must be highly accurate. For resolutions of 10 bits or higher, it is very difficult to match the comparator offset requirements. Digital correction technique relaxes the offset requirement of the comparators to a great degree [11],[12].

To build pipelined ADCs with a large tolerance to component errors, redundancy is introduced by making the sum of the individual stage resolutions greater than the resolution of the ADC. The overlapped quantization regions are eliminated by the

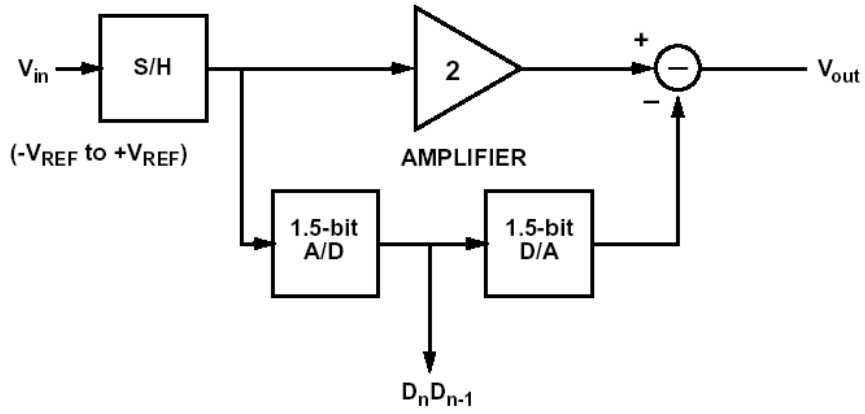


Figure 3.10: 1.5 bit pipelined ADC stage.

Sub-ADC	Sub-DAC	Stage Output
D_nD_{n-1}	$V_{dac,out}$	V_{out}
00	$-V_{ref}$	$2V_{in} + V_{ref}$
01	0	$2V_{in}$
11	V_{ref}	$2V_{in} - V_{ref}$

Table 3.1: 1.5-bit Sub-ADC and Sub-DAC outputs.

digital correction algorithm, reducing the comparator offset, nonlinearity and gain errors [10].

An architecture that adds the digital error correction to the 1-bit per stage topology with the minimum number of additional comparators is the 1.5-bit per stage pipeline topology. A 1.5-bit per stage pipelined ADC stage is shown in Figure 3.10.

thermometer code	binary code
00	00
01	01
11	10

Table 3.2: Thermometer - binary code conversion table.

In a 1.5-bit/stage configuration, each Sub-ADC consists of 2 comparators. The comparators' reference voltage levels are $V_{ref}/4$ and $-V_{ref}/4$. The 1.5-bit Sub-ADC and Sub-DAC produce 3 possible outputs and these outputs along with the stage output are shown in Table 3.1. As it can be seen from the table, the output of the Sub-ADC is in thermometer code.

The output of the 1.5-bit stage is shown in Figure 3.11. As it is apparent from the figure, for reasonable amounts of comparator offset or charge injection, the output of the stage will not over-range the following stage's resolvable input range. To linearize the transfer characteristic of the pipelined ADC, each thermometer code should be converted to binary code as shown in Table 3.2. After the conversion, the LSB of the stage is aligned with the MSB of the following stage and all the resulting bits are added to generate the final output word.

A switched capacitor (SC) implementation of the 1.5-bit stage is shown in Figure 3.12. In this implementation, the Sub-ADC consists of two comparators and the Sub-DAC is realized using an analog multiplexer.

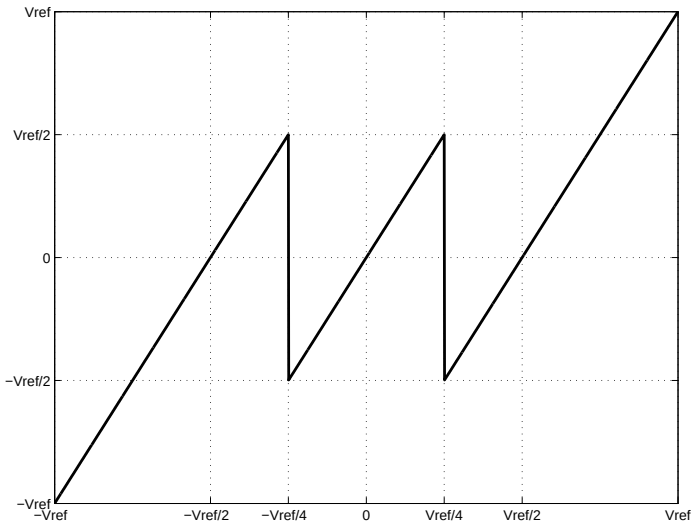


Figure 3.11: 1.5 bit pipelined ADC stage output.

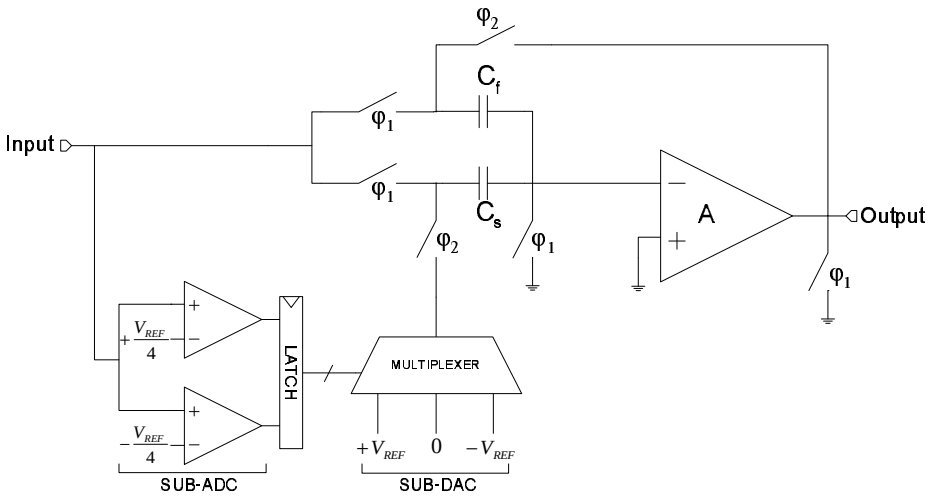


Figure 3.12: SC Implementation of 1.5-bit pipelined stage.

CHAPTER 4

THE RECONFIGURABLE PIPELINED ADC ARCHITECTURE

4.1 Overview

In this chapter, the reconfigurable pipelined ADC architecture is introduced. The system level design of the reconfigurable ADC, modes of operation and timing issues are presented and the ways for implementing the novel ADC architecture are investigated.

4.2 System Level Design

To realize a reconfigurable pipelined ADC, the initial design must satisfy the maximum speed and resolution requirements. Reconfiguration can then be employed for power scaling proportional to the effective sampling speed.

To understand the reconfiguration concept it should be noted that a cyclic ADC, when unraveled into concurrent processing stages leads to a simple pipeline design [13]. The cyclic ADC uses the same algorithm as the pipelined ADC and converts the analog input signal to a digital value by continuously generating the quantization error (residue) in one stage. When the maximum sampling speed is not required, some

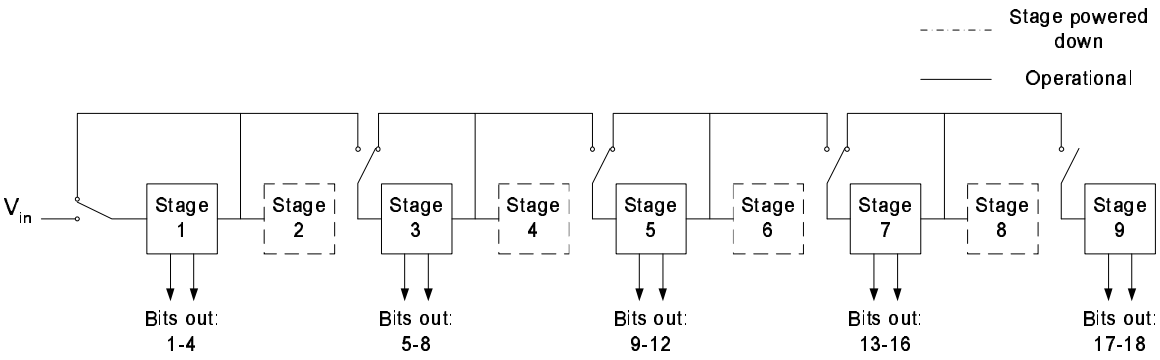


Figure 4.1: An illustration of the reconfigurable ADC architecture

stages of the pipeline can be powered down and remaining stages can be operated as pipeline-cyclic hybrids to save power.

A block diagram of the reconfigurable ADC is shown in Figure 4.1. In the case shown, a 9 stage 10-bit pipelined ADC is operated at 2/3 of the maximum operating speed and each operational stage contributes 4 bits to a total of 18 bits, except the last stage which always contributes 2 bits. Stages 1, 3, 5, 7 and 9 are fully operational and stages 2, 4, 6 and 8 are powered down. In 2/3 speed operation each of the recycling stages operate 1.5 times faster than the effective sampling frequency.

4.3 Capacitor Reuse Technique

4.3.1 Motivation

The reconfiguration approach defined in Section 4.2 requires an extra sample-and-hold (S/H) amplifier. To implement the reconfigurable pipelined ADC architecture with minimal hardware overhead, a novel technique which makes use of existing hardware is needed. The proposed novel Capacitor Reuse Technique uses the existing hardware and only extra switches are needed for implementation.

4.3.2 Modified 1.5-bit stage

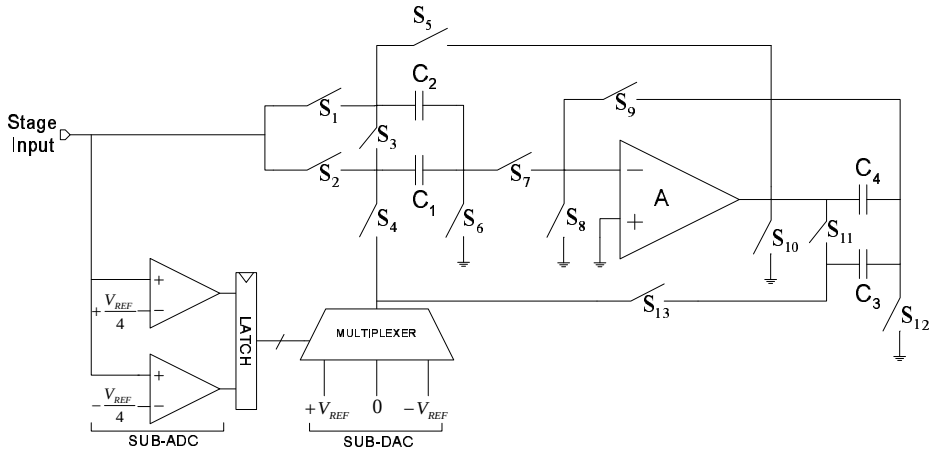


Figure 4.2: Modified SC ADC stage to realize both cyclic and pipelined operation

The 10-bit ADC designed in this work is based on a 1.5-bit/stage pipeline architecture with nine stages [9], [10], [11]. By redesigning the standard 1.5-bit pipeline stage, cyclic and reconfigurable operation is realized without the need for and extra S/H amplifier. For easier demonstration, a single ended version of the modified 1.5-bit stage is shown in Figure 4.2. As it can be seen from the figure, only extra switches and a pair of capacitors are needed for reconfigurable operation. As it will be shown in the following sections, the pair of capacitors are also redundant.

4.3.3 Clocking Scheme

For reconfigurable operation without using an extra S/H amplifier, three non-overlapping clock phases, one sampling and two amplification, are required (Figure 4.3). The operation of the reconfigurable stage during one of the low-speed modes is as follows.

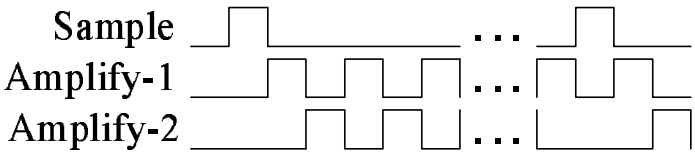


Figure 4.3: Clock phases required for reconfigurable operation.

Sampling Phase: OTA output is reset to mid-rail voltage and analog input signal is sampled on capacitors C_1 and C_2 at the end of this phase. (Figure 4.4.a).

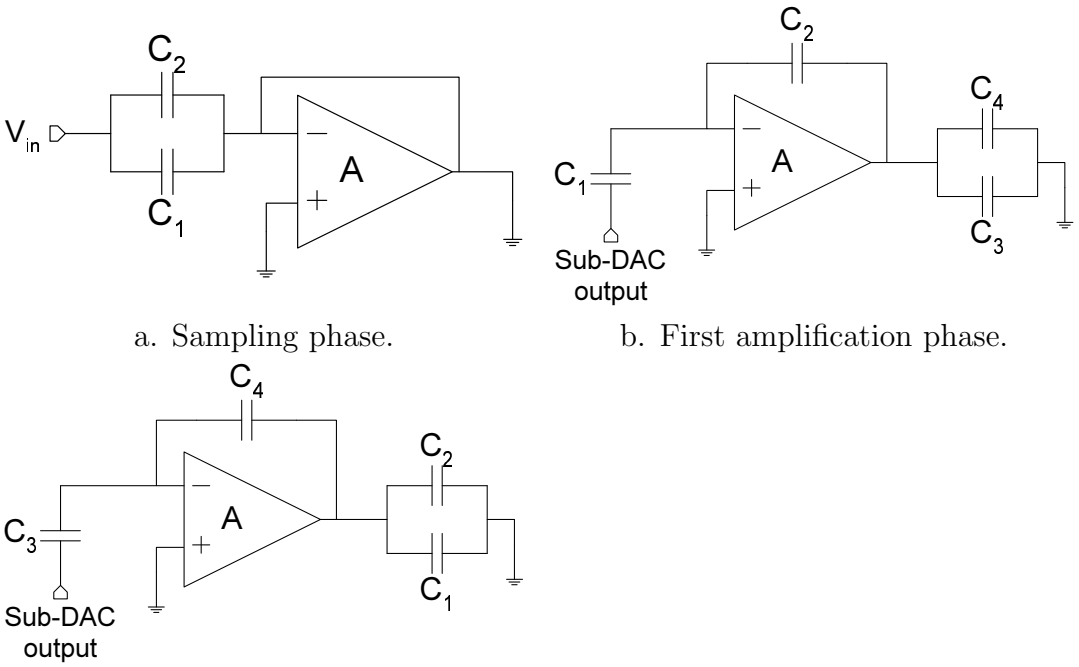
First amplification phase: C_2 closes the negative feedback loop around the OTA and the top plate of C_1 is switched to the output of the Sub-DAC. Sub-ADC generates 2-bits which are fed into the digital correction block. The generated output residue is stored on following stage's capacitors C_3 and C_4 at the end of this phase (Figure 4.4.b).

Second amplification phase: Sub-ADC generates 2-bits and the capacitors C_1 and C_2 are connected between the OTA output and ground. Also during this phase C_4 closes the negative feedback loop, the top plate of C_3 is switched to the Sub-DAC output and the generated residue is sampled on C_1 and C_2 (Figure 4.4.c).

After the initial sampling phase, depending on the mode of operation, the pipeline alternates between the first and second amplification phases for a specific number of cycles before returning to the sampling phase to acquire new input signal.

4.3.4 Capacitor Reuse Technique

Due to the digital correction, offset requirements are relaxed and dynamic comparators are used to reduce power consumption. However, dynamic comparators need to be reset for every comparison, therefore during low-speed operation for continuous generation of output bits from a single stage, Sub-ADC and Sub-DAC of the following



a. Sampling phase.

b. First amplification phase.

c. Second amplification phase.

Figure 4.4: Three phases for reconfigurable operation.

powered-down stage are utilized during the second amplification phase. Also this approach lets us to use the sampling capacitors from the following stage, which removes the need for an extra pair of capacitors which is shown in Figure 4.2.

In this design, odd-numbered (1, 3, 5, 7) and even-numbered (2, 4, 6, 8) stages are topologically different because in any of the low-speed operation modes all the even-numbered stages are powered down and only some of the odd-numbered stages operate in cyclic fashion. During low-speed operation, if the stage $2n-1$ (where $n = 1, 2, 3, 4$) is operational, the capacitors, Sub-ADC and Sub-DAC of the following even-numbered stage, stage $2n$, are used to save area, while the OTA of the even numbered stage is powered down. The last stage is a true 2-bit stage, which consists of 3 comparators and conversion logic. In any operation mode, the last quantization must always be

Operation Mode	Ratio	Effective Sampling Rate	Stages Operational
1	1	20 MHz	All
2	2/3	13.33 MHz	1-3-5-7-9
3	2/4	10 MHz	1-3-5-9
4	2/5	8 MHz	1-3-9
5	2/6	6.67 MHz	1-3-9
6	2/7	5.71 MHz	1-3-9
7	2/8	5 MHz	1-8-9
8	2/9	4.44 MHz	1-9

Table 4.1: Reconfiguration modes of the pipelined ADC.

performed by a true 2-bit stage. Therefore stage 9 is always operational regardless of the effective sampling speed. However since this stage does not contain an OTA, overall power consumption figures are not significantly affected.

4.3.5 Available Modes of Operation

The modes of operation that are realizable with the reconfigurable pipelined ADC are shown in Table 4.1. In standard pipelined operation the sampling speed is 20 MHz, which is the maximum achievable sampling speed with the reconfigurable pipelined ADC. Total number of operation modes that are achievable is equal to $N - 1$, where N is the total number of stages.

As explained in Section 4.3.4 and apparent from Table 4.1, the last stage, which is a true 2-bit stage, is always operational regardless of the mode of operation.

Operation Mode	Stages	Number of resolved bits
1	All	2
2	1,3,5,7	4
3	1,3	6
	5	4
4	1,3	8
5	1	10
	3	6
6	1	12
	3	4
7	1	14
	8	2
8	1	16

Table 4.2: Number of resolved bits for each stage during different modes of operation.

In mode 7; stage 8, which is an even-numbered stage is operational, but because of the operation of the reconfigurable pipeline, stage 8 is only resolving 2 bits out of 18 bits and operates as a standard pipeline stage. The number of bits resolved in each mode of operation by each stage except stage 9 are shown in Table 4.2.

The choice of number of stages to be used for the speed ratio $\frac{2}{M}$ for an N bit reconfigurable pipelined ADC with digital correction is given by

$$\lceil \frac{2N-4}{2M-2} \rceil + 1 \tag{4.1}$$

Clock name	Operation
ϕ_1	Sampling phase
ϕ_2	First amplification phase
ϕ_3	Second amplification phase

Table 4.3: Clocking Signals.

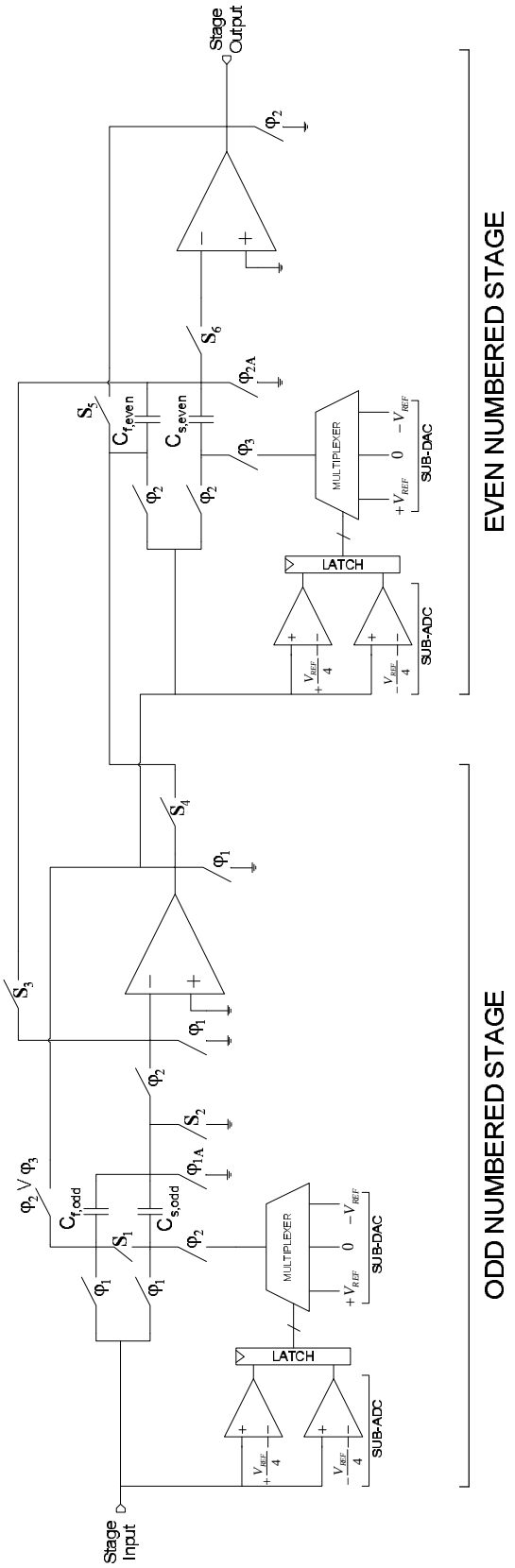
where $\lceil\rceil$ is the ceiling function and the addition of 1 stems from the fact that the last stage is always operational.

4.4 Clocking Signals

A pair of consecutive odd and even numbered stages is shown in Figure 4.5. Clocking signals in the figure can be interpreted as shown in Table 4.3. Also clocking signals for 5 modes of operation are shown in Figure 4.6 as an example. Charge injection effects were removed using advanced clocks, which are denoted by an 'A' subscript.

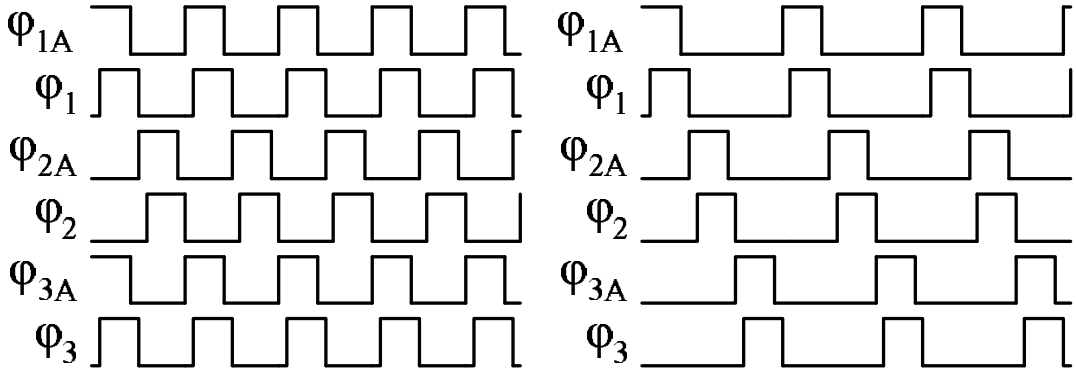
In Figure 4.5 switches S_1, S_2, S_3 and S_4 are turned off during full-speed mode and switches S_5 and S_6 are turned off during one of the lower-speed modes. When they are on, switches S_1, S_3, S_4 and S_5 are clocked by ϕ_3 and S_2 is clocked by ϕ_{3A}. Switch S_6 is turned on or off depending on the mode. Figure 4.5 with the clock signals for one of slow-speed modes is shown in Figure 4.7.

At full-speed, the analog signal to be resolved is sampled by the odd numbered stage during ϕ_1. During ϕ_2, the capacitor $C_{f,odd}$ closes the negative feedback loop



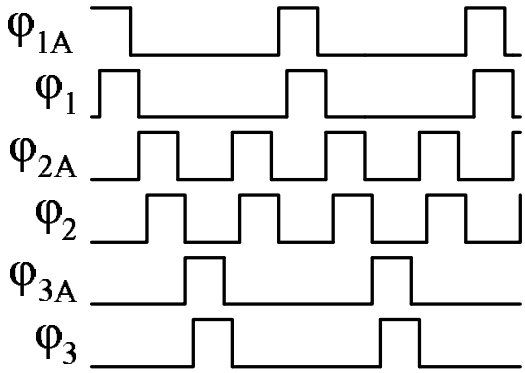
36

Figure 4.5: Pair of consecutive ADC stages.

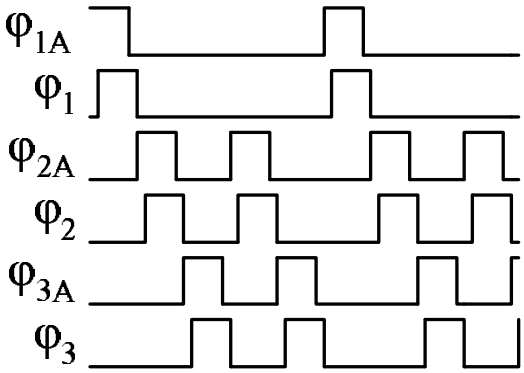


a. Mode-1

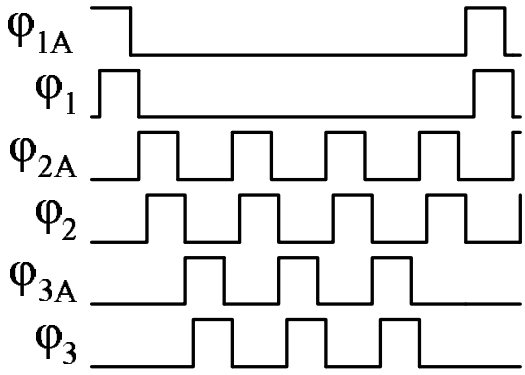
b. Mode-2



c. Mode-3



d. Mode-4



e. Mode-7

Figure 4.6: Clock signals for different reconfiguration modes.

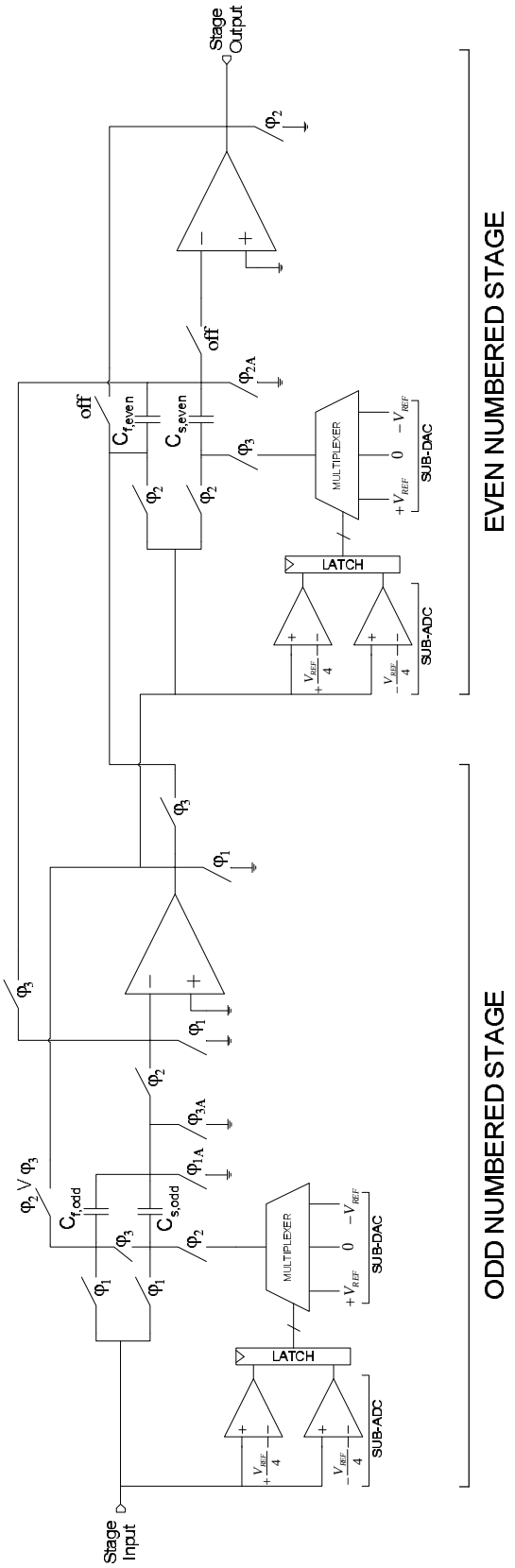


Figure 4.7: Pair of consecutive ADC stages.

around the OTA, and the residue is generated. As it is generated, the residue is sampled by the capacitors of the following even-numbered stage ($C_{s,even}$ and $C_{f,even}$).

In one of the slower modes, the operation during ϕ_1 and ϕ_2 phases is the same, however during the ϕ_3 phase, the bottom plate of $C_{s,even}$ is connected to the Sub-DAC output of the even-numbered stage and top plate of the same capacitor is connected to the OTA input of an odd-numbered stage. Additionally $C_{f,even}$ closes the negative feedback loop around the OTA and the generated residue is sampled on the capacitors of the odd numbered stage ($C_{s,odd}$ and $C_{f,odd}$) during this phase. Depending on the mode of operation; either the residue sampled on the odd numbered stage capacitors is used for new residue generation, or a new analog value from the previous stage is sampled.

CHAPTER 5

DESIGN EXAMPLES AND SIMULATION RESULTS

5.1 Overview

In this chapter circuit level design of the reconfigurable ADC is presented. Main circuit blocks and their designs are explained. Memory effect,which is present during low speed operation is also demonstrated. The designed circuits and the reconfigurable ADC was simulated in AMI 0.5u CMOS process and with a 3.3 V voltage supply. Chosen maximum conversion speed was 20MHz. Simulation results are shown to verify the performance of the proposed reconfigurable ADC architecture.

5.2 Main Circuit Blocks

5.2.1 Operational Transconductance Amplifier

To achieve 10-bit resolution, a 9-stage, 1.5-bit/stage digitally corrected pipeline architecture was used. Maximum voltage swing at the each S/H amplifier output was chosen to be 0.3V to minimize non-linearity. This translated to 0.6V differential peak-to-peak output voltage.

For the chosen speed and resolution, the open loop gain and Gain-Bandwidth Product (GBW) requirements for the S/H amplifier are calculated as follows:

$$T_{settle} = \frac{1}{2} T_{sample,max} = 25ns \tag{5.1}$$

For linear settling to $\frac{1}{2}LSB$ accuracy, settling time must be

$$7.6\tau = 25ns \tag{5.2}$$

and

$$\tau = 3.29ns \tag{5.3}$$

The GBW requirement of the S/H amplifier is calculated using equation 5.4 and found to be 48.38 MHz. But because of the parasitic capacitances of the circuit, this value needs to be higher.

$$GBW = \frac{1}{2\pi\tau} \tag{5.4}$$

For interstage gain error less than 0.5 LSB, the open loop gain of the OTA should be

$$A_{openloop} \geq 2 \cdot 2^{N+1} = 72dB \tag{5.5}$$

where N is equal to the ADC resolution.

A fully-differential telescopic OTA, as shown in Figure 5.1, was used as the S/H amplifier in the first eight stages. Telescopic OTA topology was chosen as the amplifier in the pipelined stages for its robust design and good gain and frequency response. No capacitor scaling was employed and thus no amplifier design changes were necessary. Switches were added to OTA's biasing circuitry to power it down when required. The designed OTA's targeted gain was 72 dB and phase margin was 60 degrees for good settling performance. The gain and phase plots of the OTA for different

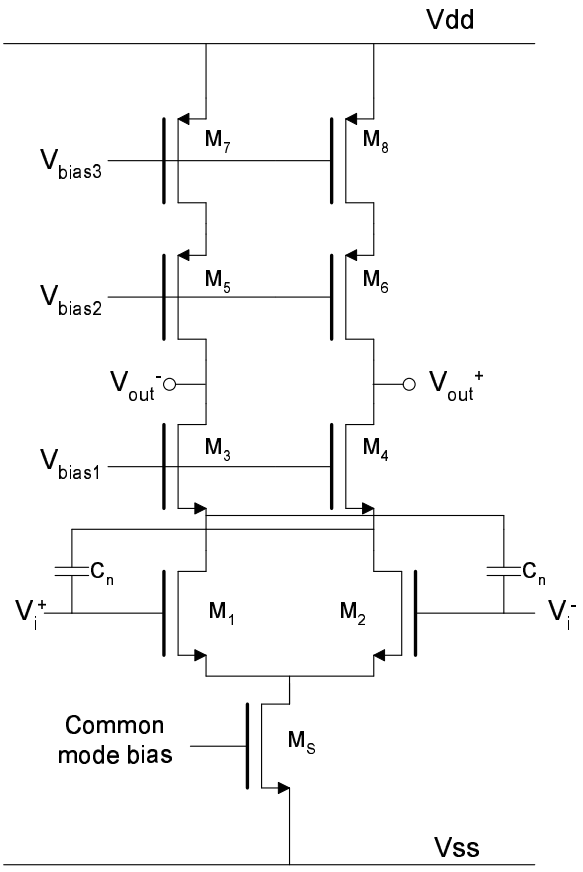


Figure 5.1: Fully differential telescopic OTA used in the ADC stages.

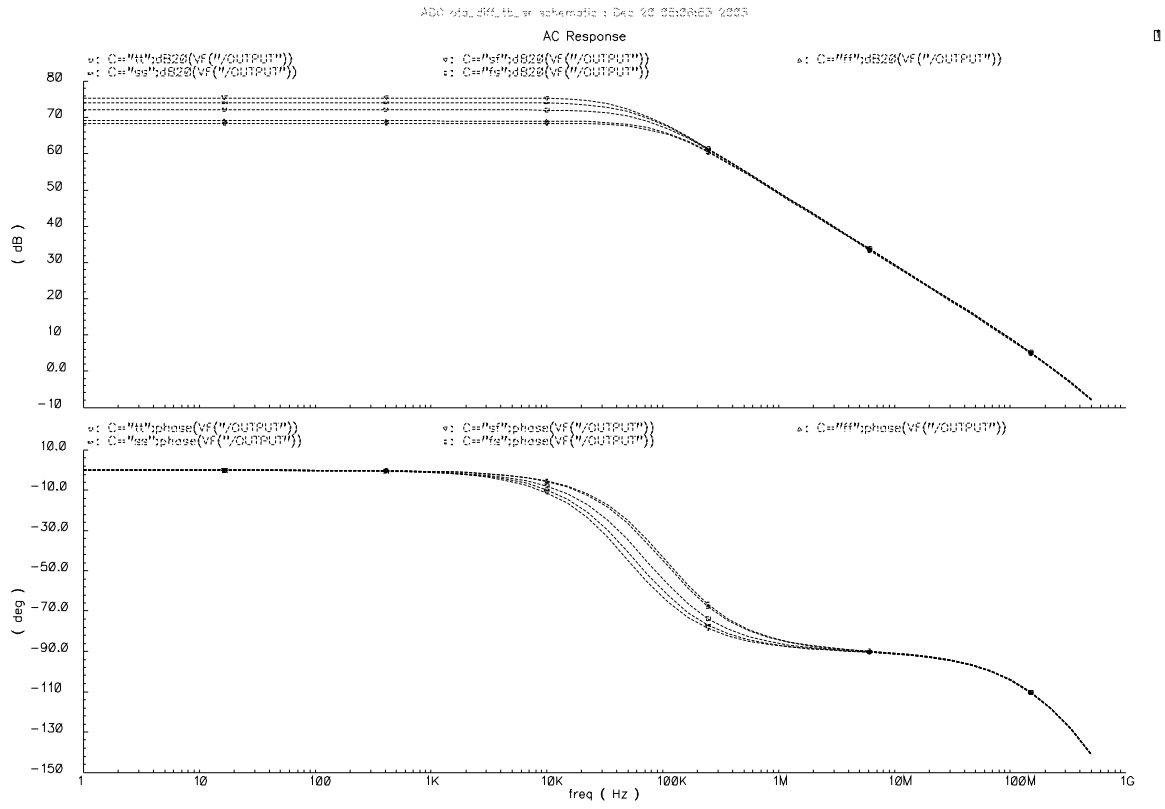


Figure 5.2: Gain and phase response of the OTA for different simulation corners.

simulation corners is shown in Figure 5.2. Also the overall OTA performance at different simulation corners is summarized in Table 5.1. The designed OTA's power consumption is 2.608 mW for typical simulation corner.

To decrease the effect of input capacitance of the OTA on the performance of the ADC, neutralization capacitors were used [20]. The differential capacitance looking into the OTA input without the cancellation capacitances is

$$C_{in} = C_{gs1} + C_{gd1}(1 - A_{gd1}) \tag{5.6}$$

where C_{gs1} and C_{gd1} are gate-to-source and gate-to-drain capacitances of the input transistor, respectively, and A_{gd1} is the small-signal gain from the gate to drain of

Corner	DC Gain (dB)	Phase Margin	GBW	Settling Time	Slew Rate
ff	69.08	60.04	289.3MHz	18.55ns	86.35M
fs	68.44	60.12	284.1MHz	20.26ns	86.92M
sf	75.33	59.52	297.4MHz	20.29ns	82.81M
ss	74.02	59.45	296.6MHz	20.97ns	82.66M
tt	72.12	59.7	293.6MHz	20.19ns	84.4M

Table 5.1: OTA performance for different simulation corners.

transistor M_1. When neutralization capacitors are taken into consideration, the input capacitance is given by

$$C_{in} = C_{gs1} + C_{gd1}(1 - A_{gd1}) + C_n(1 + A_{gd1}) \tag{5.7}$$

where C_n is the neutralization capacitance. By choosing the appropriate values for C_n, the effect of the OTA input capacitance on the overall ADC performance can be decreased.

5.2.2 Common-mode Feedback Circuit

Because a fully-differential OTA is used as the S/H amplifier, a common-mode feedback circuit is required to maintain the correct common-mode voltage at the output of the OTAs.

The reconfigurable operation requires the correct common-mode voltage level for a single OTA to be maintained during successive amplifications. If a stage is operational in one of the low-speed modes, the OTA is always amplifying and is not reset until the input signal is sampled. To solve this problem, a switched capacitor (SC) common-mode feedback circuit (CMFB), as shown in Figure 5.3, is designed. In this circuit,

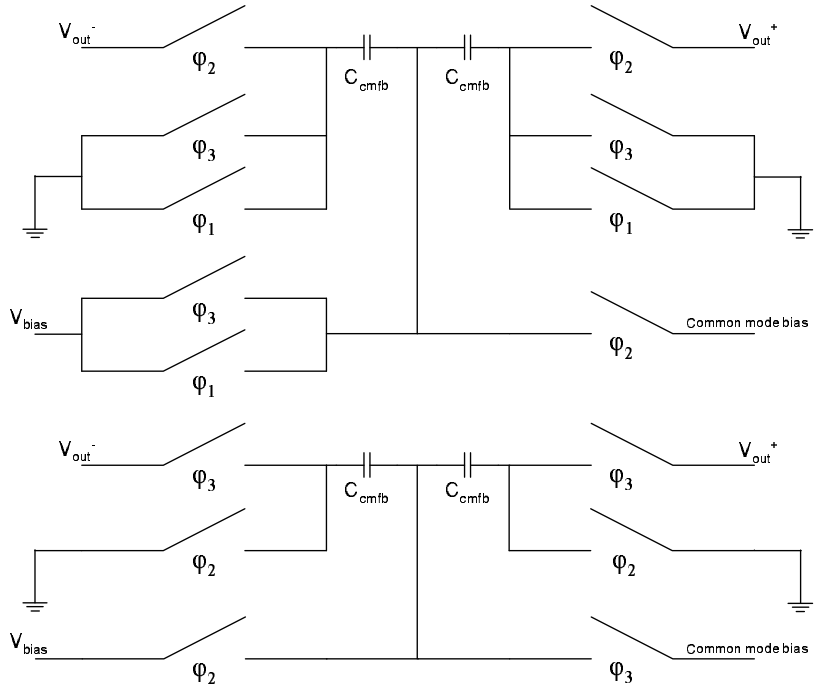


Figure 5.3: Enhanced CMFB for recycling operation.

when one pair of capacitors is supplying the biasing voltage to the OTA, the same biasing voltage is stored on the other pair for next phase of operation.

5.2.3 Dynamic Comparator

The comparator used in the ADC was introduced in [9], and it is made of simple dynamic latches to remove DC power consumption. Because digital correction is employed, comparator offsets up to $V_{ref}/4$ can be tolerated. The lower set of NMOS transistors are biased in triode region and they act as variable resistor elements. The threshold level of the comparator is given by

$$V_{th} = \frac{W_1}{W_2} \cdot V_{ref} \tag{5.8}$$

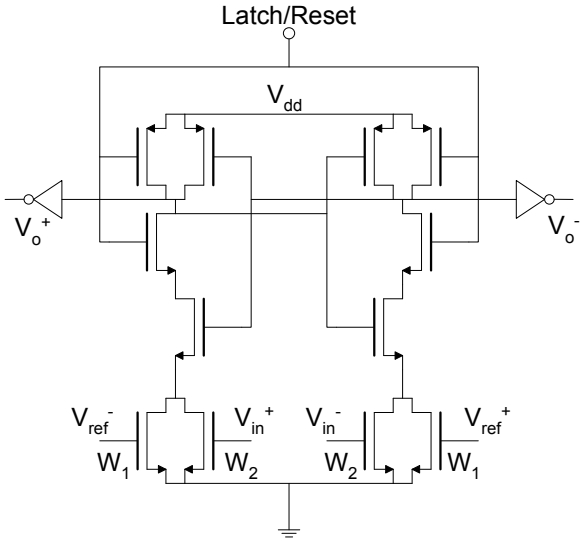


Figure 5.4: Dynamic comparator with controllable threshold level.

where W_1 and W_2 are the widths of the reference and input transistors, respectively. The desired threshold voltage levels $\pm V_{ref}/4$ can be achieved with the ratio $W_1/W_2 = 1/4$ and changing the reference voltage polarities accordingly. Because the dynamic latches are prone to large offset voltages if the loads are mismatched, basic CMOS inverters were implemented at the output of the comparator to balance the capacitive loads (Figure 5.4).

5.3 Memory Effect

When the reconfigurable ADC is working in one of the lower-speed operation modes, the charges remaining on the capacitors are not discharged as in the standard pipelined operation, thus effectively increasing the settling time and rise time for some input voltage values. Because of the memory effect, the maximum conversion

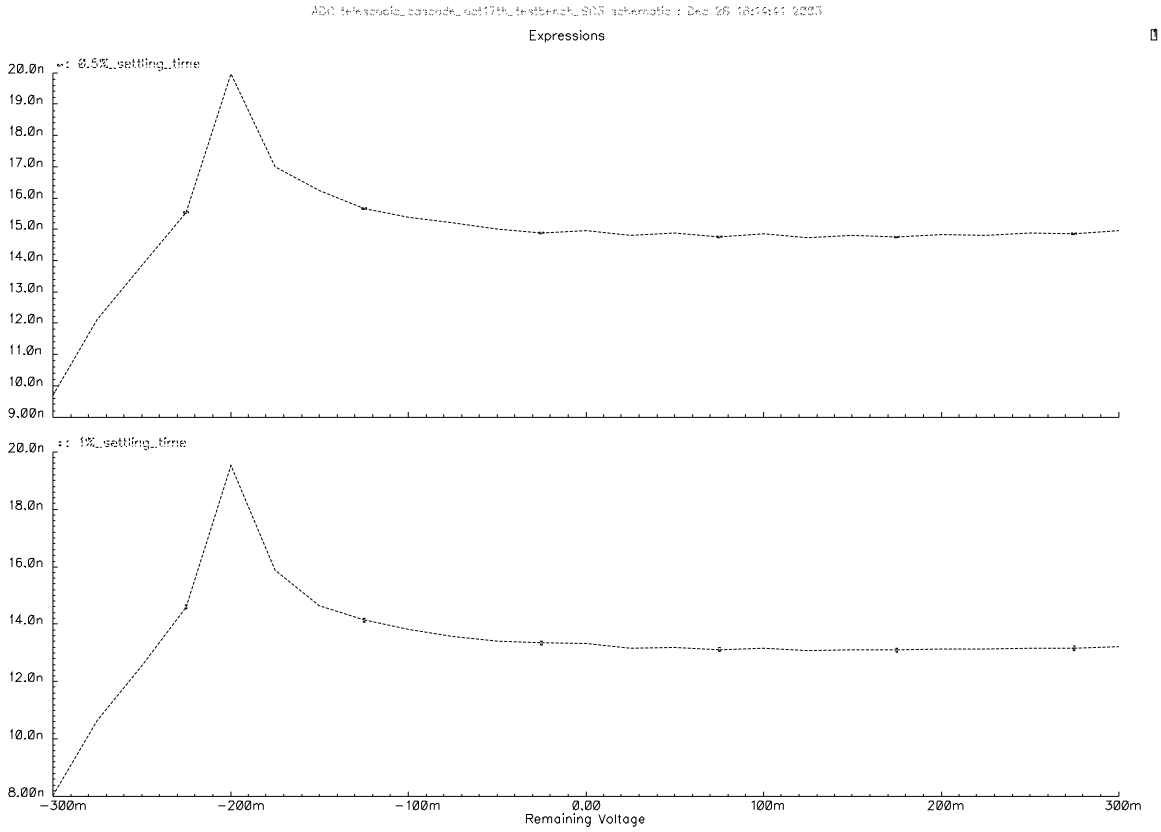


Figure 5.5: Settling time variation for an input value of 100mV.

speed achievable by a basic pipelined ADC implemented in the same process cannot be achieved by a reconfigurable pipelined ADC using the same S/H amplifier.

Simulation results for different input voltage values and different amounts of remaining charge on the capacitors are shown in Figure 5.5 and Figure 5.6. As it is apparent from the plots, settling time performance varies for different input voltage values. Best overall settling performance can be achieved by fully discharging the capacitors because for the worst case the voltage difference that needs to be overcome will be at most 300mV as opposed to 600mV.

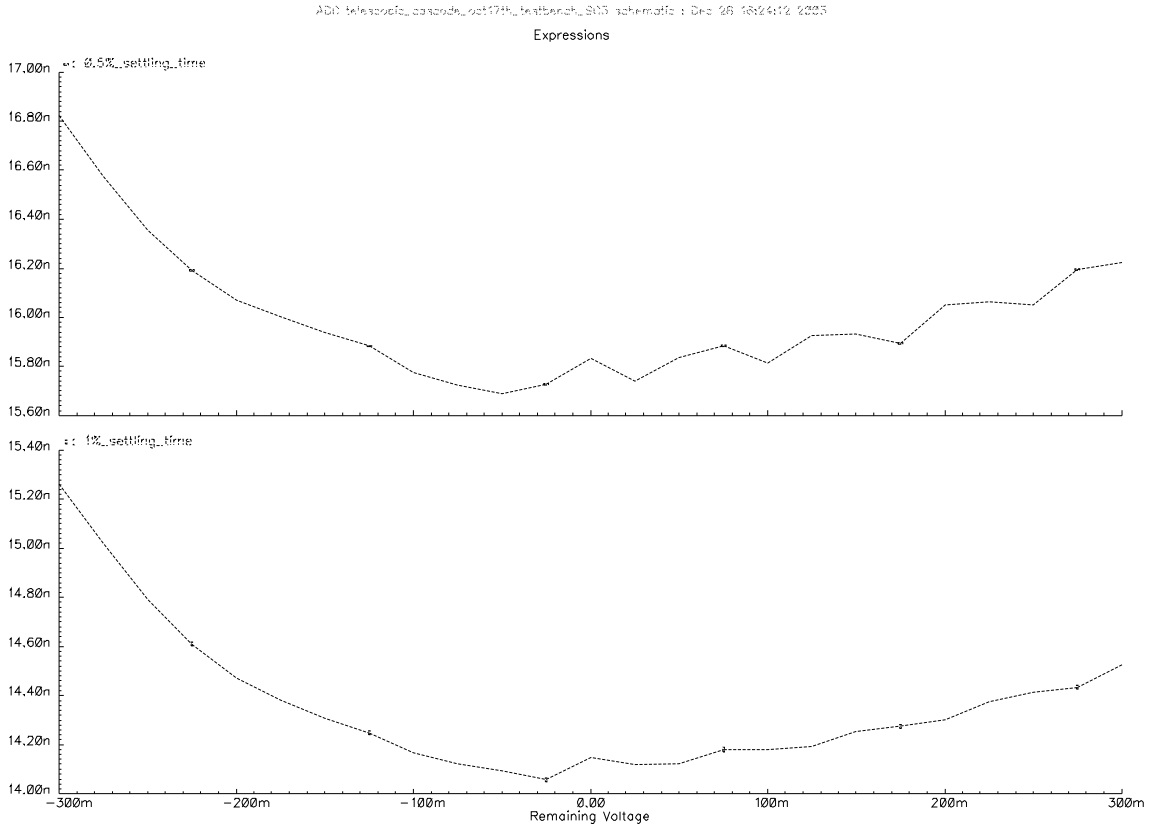


Figure 5.6: Settling time variation for an input value of 200mV.

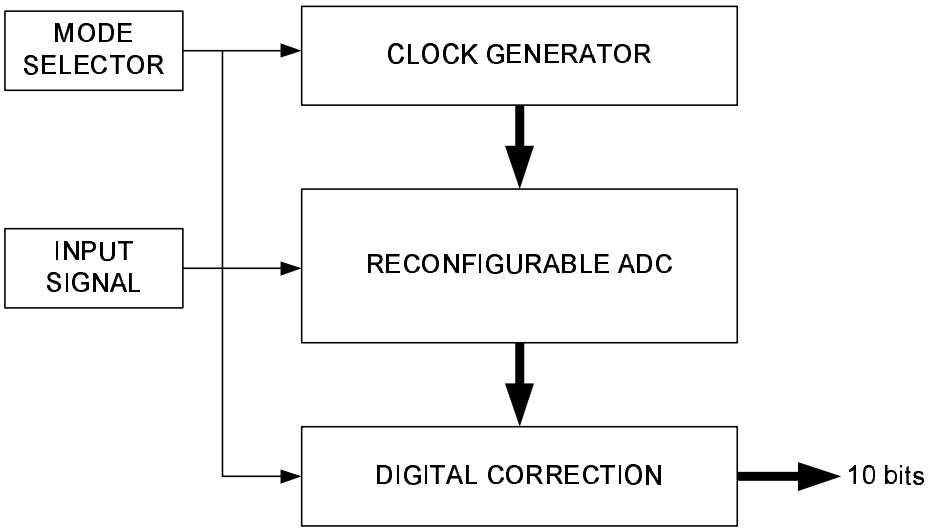


Figure 5.7: Simulation testbench.

5.4 Simulation Results

In this section simulation results for 5 modes of operation are presented to prove the concept of reconfiguration with linear power-speed scaling. Both static and dynamic parameters were found through transient simulations. The design has been simulated in a 0.5μm CMOS technology.

5.4.1 Simulation Setup

The simulation testbench is shown in Figure 5.7. The Mode Selector, Clock Generator and Digital Correction blocks have been implemented using Verilog. By changing the mode parameter in the Verilog code of the Mode Selector block, control signals for the Clock Generator and the Digital Correction blocks are created and reconfigurable operation is realized.

Operation Mode	Max. DNL	Max. INL
1	0.56	0.67
2	0.58	0.68
3	0.61	0.81
4	0.58	0.79
7	0.56	0.66

Table 5.2: Static performance of the ADC for different modes.

The reconfigurable ADC block is fully implemented at the circuit level and transient simulations were run to calculate both dynamic and static parameters. Simulations for each mode of operation took more than twenty four hours. During dynamic parameters calculation, before taking the FFT of the output signal Blackman window was applied to the signal to minimize spectral leakage. Dynamic parameters for all modes of operation were calculated using 1024 point FFT data.

5.4.2 Static Parameters

For static parameter simulations, a slowly rising ramp was applied to the ADC input and static parameters was calculated.

Figure 5.8 shows the typical plots for the differential nonlinearity (DNL) and integral nonlinearity (INL) errors of the ADC when operating in full-speed mode. The static parameters for all the configuration modes are summarized in Table 5.2.

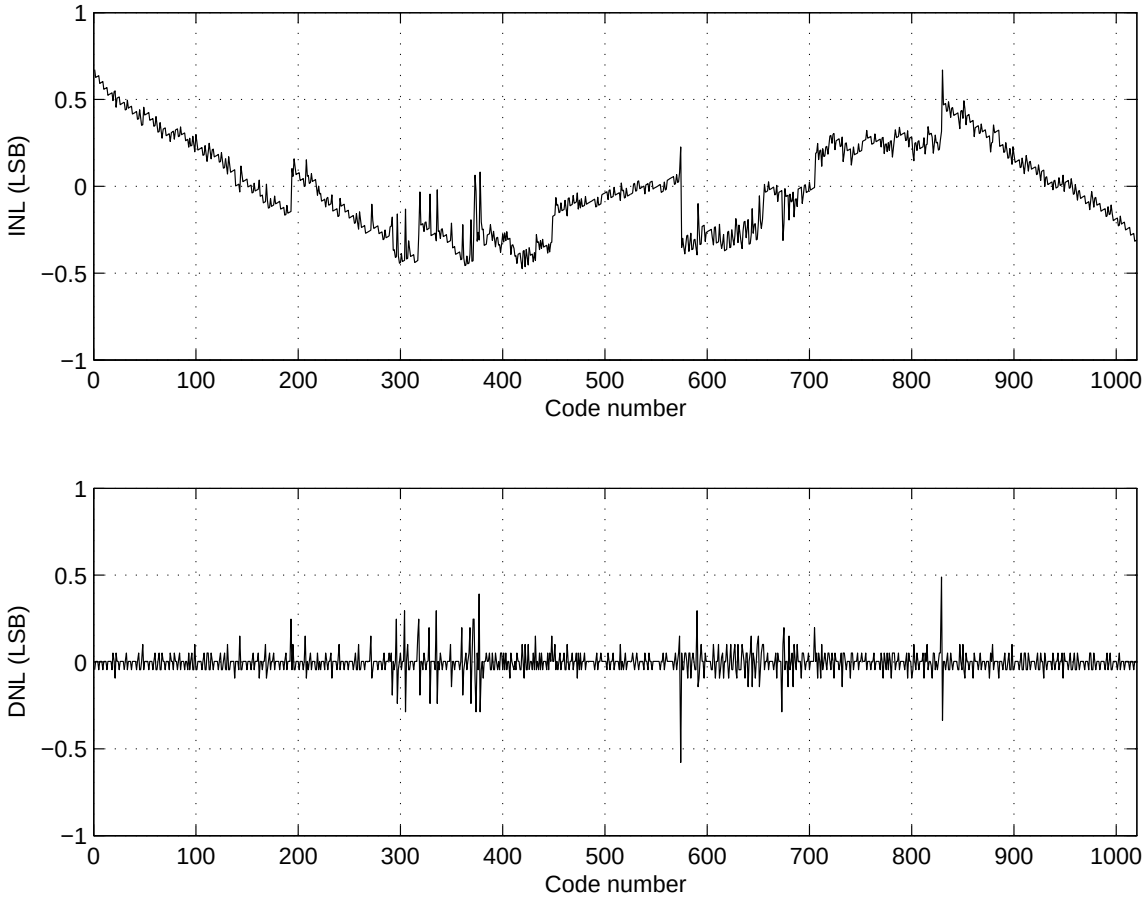


Figure 5.8: INL and DNL plots for full-speed operation.

Operation Mode	SNR	SNDR	SFDR	THD	ENOB
1	62.04	61.81	74.77	-74.68	9.97
2	60.08	59.65	74.00	-69.83	9.62
3	59.43	59.07	71.23	-70.02	9.52
4	60.14	59.92	76.53	-72.93	9.66
7	60.46	60.10	71.68	-71.05	9.69

Table 5.3: Dynamic performance of the reconfigurable ADC.

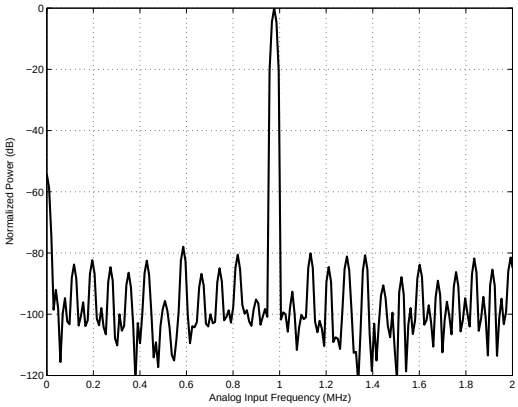
5.4.3 Dynamic Parameters

The dynamic performance of the ADC for reconfigurable operation is presented in Figure 5.9, where a full-scale input sinewave at $f_{in} = 976.56$ kHz is applied to the ADC input.

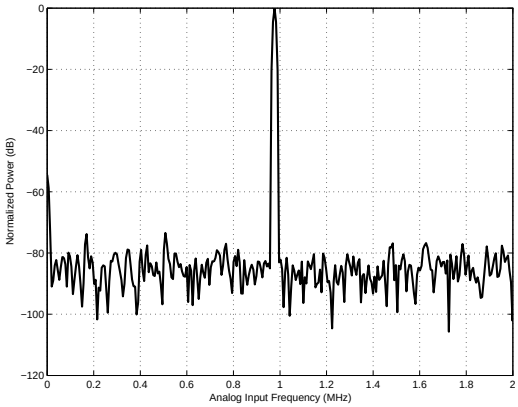
The overall dynamic performance of the reconfigurable ADC for all modes is summarized in Table 5.3. ENOB for any one of the lower-speed operations is slightly lower than full speed operation because in low-speed operation OTA is not reset between successive amplifications and suffers from memory effects.

5.4.4 Power Consumption

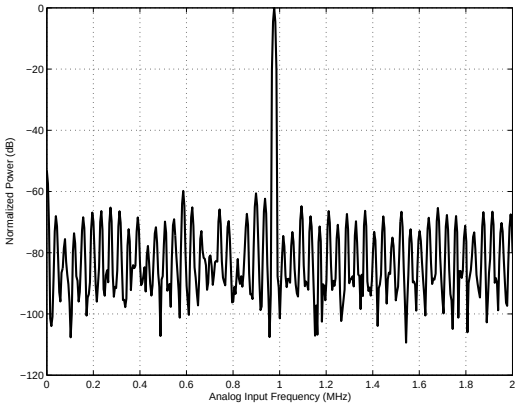
Figure 5.10 shows the actual and expected power consumption after powering down the unused stages. The top dashed line with triangle markers shows the power consumption scaled linearly with changing effective sampling speed. The solid line with circle markers is the simulated power consumption for different modes of operation. Finally the bottom line is the expected power consumption with regards to the number of operational stages which include a S/H amplifier from Table 4.1.



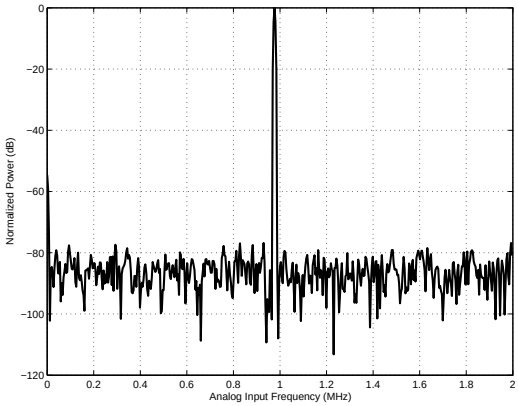
a. Mode-1



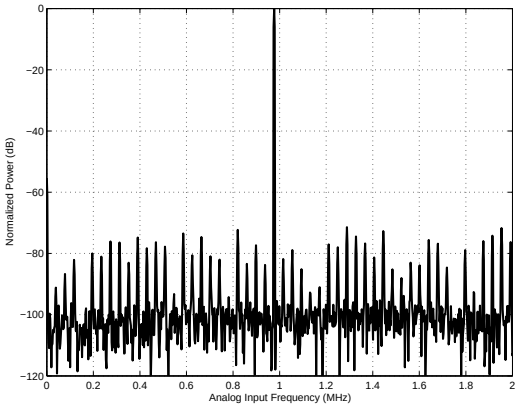
b. Mode-2



c. Mode-3



d. Mode-4



e. Mode-7

Figure 5.9: FFT plots for different reconfiguration modes.

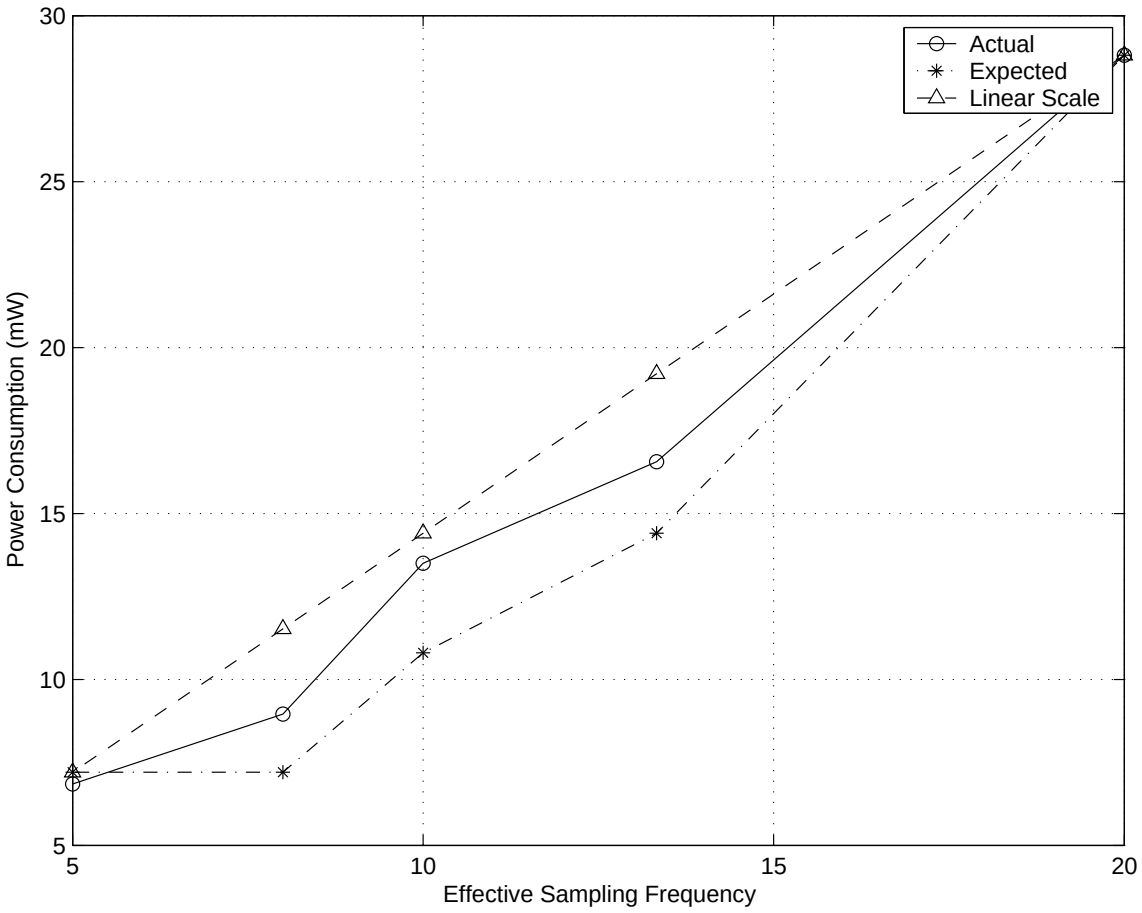


Figure 5.10: Power consumption for different modes

A comparison of the simulation results to the linearly power scaled line reveals that the proposed technique achieves better than linear power scaling performance. However, as the conversion speed decreases, eventually the ADC will operate like a single cyclic ADC which will limit the power scaling capability. After that point on, the analog power consumption will be constant and will not change with changing conversion speed.

CHAPTER 6

CONCLUSION

In this thesis, a novel design approach for low-power reconfigurable pipelined ADCs is presented. The methods for scaling power with varying sampling speed are investigated. The summary is as follows:

Pipelined ADCs offer medium-to-high speed for moderate resolution values. Employing carefully designed S/H amplifiers and sizing the sampling capacitors of the pipelined stages carefully, the power consumption can be minimized.

Due to the nature of the pipelined operation, resolution and power can be scaled linearly, but it is not straightforward to scale power linearly with sampling speed. Noticing the fact that each pipelined stage can work independently as a cyclic ADC with the addition of an extra S/H amplifier, a new type of reconfigurable pipelined ADC can be implemented. Thus low-power reconfigurable operation can be realized by keeping only the required number of stages operational to save power without any decrease in the resolution of the ADC. A novel technique for designing reconfigurable pipelined ADC stages is also presented to minimize the amount of additional hardware and power consumption.

A 10-bit resolution reconfigurable pipelined ADC with maximum conversion speed of 20MS/s is simulated using AMI 0.5u 2-poly, 3-metal CMOS process. Simulations

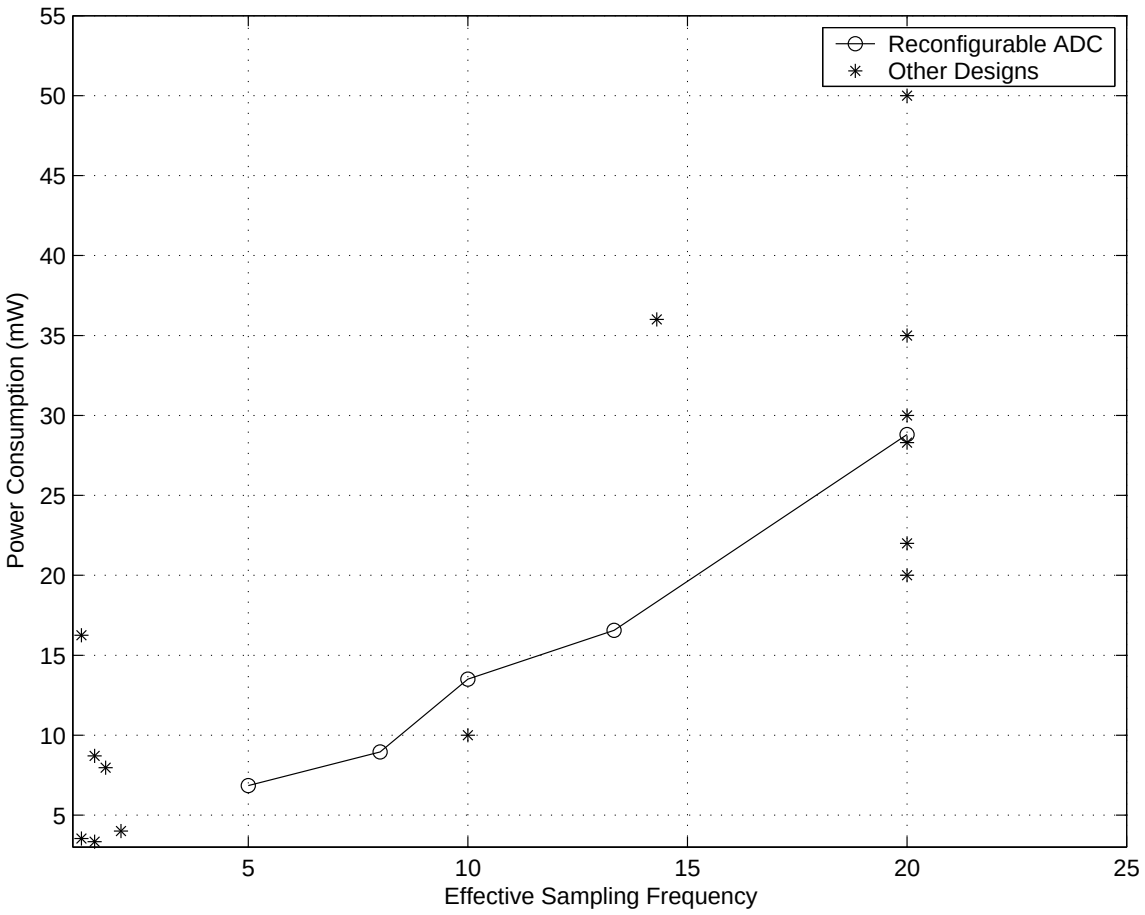


Figure 6.1: Power comparison of the designed ADC with other designs.

show that the ENOB varies between 9.52 and 9.97 and power consumption is 28.8mW for full-speed operation and 6.85mW for 1/4 speed operation.

A comparison of the designed ADC performance with other ADC designs in terms of power comparison is shown in Figure 6.1. All the ADCs shown are 10-bit ADCs designed in different processes. As it can be seen on the figure, some designs dissipate less power than the designed ADC, but all these lower-power designs are simple ADCs without any reconfiguration capability.

In order to compare the performance of the designed reconfigurable ADC with other ADCs in the literature, a figure of merit (FOM) is also used. A commonly used FOM based on the conversion speed (f_s), ENOB and power dissipation (P) is used for computing the FOM and it is given by

$$FOM = \frac{2^{ENOB} f_s}{P} \tag{6.1}$$

For a better performing ADC, the calculated FOM value should be higher. Figure 6.2 displays the calculated FOM for the designs shown in Figure 6.1. The FOM line for the reconfigurable ADC is not straight as expected because of the changing ENOB values for different modes of operation.

6.1 Recommendations for Further Work

Based on the analysis and the simulation results, further work needed to improve the reconfigurable ADC is summarized as follows:

The memory effect present during the lower-speed operation is briefly demonstrated through the simulation results. The solutions for the memory effect, which limits the performance of the OTA and the whole pipeline, should be investigated to further improve the performance of the reconfigurable pipelined ADC. Redesigning the OTAs for better performance is a solution for this problem but even with better performance OTAs and consuming more power, the achievable maximum conversion speed will not be reached due to the topology and the operation of the reconfigurable pipeline.

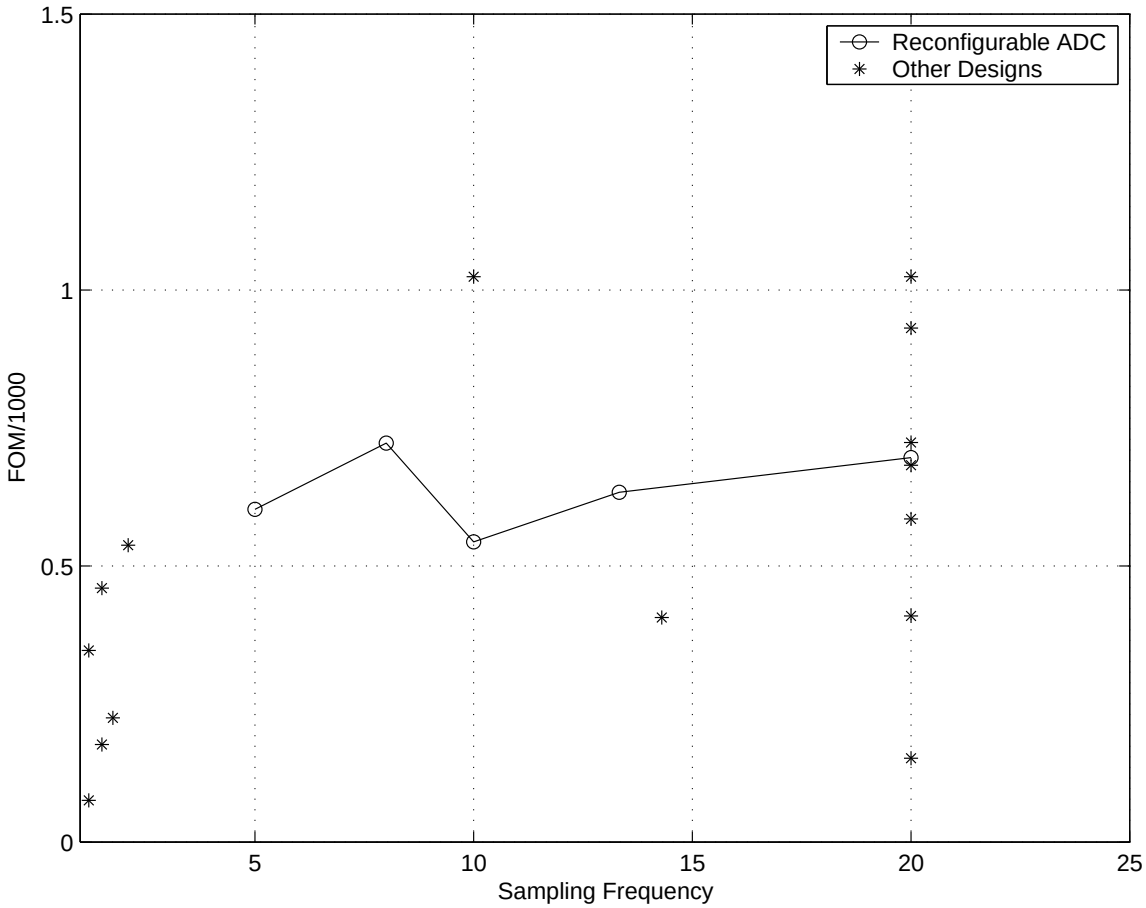


Figure 6.2: FOM vs sampling frequency.

The Verilog code written for realizing the clock generation circuitry is behavioral and cannot be synthesized. Further work needs to be done for writing fully-synthesizable Verilog code for the clock generation circuit.

Analog and digital calibration techniques have been used for increasing the resolution of the ADCs. Analog calibration techniques use additional analog hardware whereas the digital calibration techniques employ post processing which can be integrated with the reconfigurable ADC without any additional hardware. Further work should be done to investigate the ways for integrating the reconfigurable pipelined ADCs with digital calibration architectures. Although the digital circuit complexity will increase with the addition of the digital calibration, it is the only way for achieving accuracy greater than 10-bits.

BIBLIOGRAPHY

[1] J. Ryynanen, K. Kivekas, J. Jussila, L. Sumanen, A. Parssinen, and K. A. I. Halonen. A single-chip multimode receiver for gsm900, dcs1800, pcs1900, and wcdma. *IEEE Journal of Solid-State Circuits*, 38(4):594–602, April 2003.

[2] High-Speed ADCs Blaze Path To Host Of Performance Advances. `http://www.elecdesign.com/Articles/Print.cfm?ArticleID=5245`.

[3] M. Gustavvson, J. J. Wikner, and N. N. Tan. *CMOS Data Converters for Communications*. Kluwer Academic Publishers, 2000.

[4] A Simple ADC Comparison Matrix. `http://www.maxim-ic.com/appnotes.cfm/appnote_number/2094`.

[5] K. Gulati and H-S Lee. A low-power reconfigurable analog-to-digital converter. *IEEE Journal of Solid-State Circuits*, 36(12):1900–1911, December 2001.

[6] P. Setty, J. Barner, J. Plany, H. Burger, and J. Sonntag. A 5.75 b 350 msample/s or 6.75 b 150 msample/s reconfigurable flash adc for a prml read channel. In *Digest of Techical Papers: IEEE International Solid-State Circuits Conference*, pages 148–149, February 1998.

[7] H. Ohara, H. X. Ngo, M. J. Armstrong, and P. R. Gray. A cmos programmable self-calibrating 13-bit eight channel data acquisition peripheral. *IEEE Journal of Solid-State Circuits*, 22(6):930–938, December 1987.

[8] A. M. Abo and P. R. Gray. A 1.5-v, 10-bit, 14.3-ms/s cmos pipeline analog-to-digital converter. *IEEE Journal of Solid-State Circuits*, 34(5):599–605, May 1999.

[9] T. B. Cho and P. R. Gray. A 10 b, 20 msample/s, 35 mw pipeline a/d converter. *IEEE Journal of Solid-State Circuits*, 30(3):166–172, March 1995.

[10] S. H. Lewis, H. S. Fetterman, G. F. Gross, Jr., R. Ramachandran, and T. R. Viswanathan. A 10-b 20-msample/s analog-to-digital converter. *IEEE Journal of Solid-State Circuits*, 27(3):351–358, March 1992.

[11] S. H. Lewis and P. R. Gray. A pipelined 5-msample/s 9-bit analog-to-digital converter. *IEEE Journal of Solid-State Circuits*, 22(6):954–961, December 1987.

[12] S. H. Lewis. Optimizing the stage resolution in pipelined, multistage, analog-to-digital converters for video-rate applications. *IEEE Transactions on Circuits and Systems-II*, 39(8):516–523, August 1992.

[13] A. Savla, A. Ravindran, and M. Ismail. A reconfigurable low-power pipelined adc for multi-standard wireless applications. In *Proceedings IEE-Japan Analog VLSI Workshop*, September 2002.

[14] D. W. Cline and P. R. Gray. A power optimized 13-b 5 msamples/s pipelined analog-to-digital converter in 1.2 μm cmos. *IEEE Journal of Solid-State Circuits*, 31(3):294–303, March 1996.

[15] D. A. Johns and K. Martin. *Analog Integrated Circuit Design*. John Wiley & Sons, Inc., 1997.

[16] S. Sutarja and P. R. Gray. A pipelined 13-bit, 250-ks/s, 5 v analog-to-digital converter. *IEEE Journal of Solid-State Circuits*, 23(6):1316–1323, December 1988.

[17] R. H. McCharles, V. A. Saletore, W. C. Black, Jr., and D. A. Hodges. An algorithmic analog-to-digital converter. In *Digest of Techical Papers: IEEE International Solid-State Circuits Conference*, pages 96–97, Philadelphia, February 1977.

[18] P.W. Li, M.J. Chin, P.R. Gray, and R. Castello. A ratio-independent algorithmic analog-to-digital conversion technique. *IEEE Journal of Solid-State Circuits*, 19(6):828–836, December 1984.

[19] D. W. Cline. *Noise, Speed, and Power Trade-offs in Pipelined Analog to Digital Converters*. PhD thesis, University of California, Berkeley, 1996.

[20] P. G. Gray, P. J. Hurst, S. H. Lewis, and R. G. Meyer. *Analysis and Design of Integrated Circuits*. John Wiley & Sons, Inc., 4th edition, 2001.

[21] W. C. Song, H. W. Choe, S. U. Kwak, and B. S. Song. A 10-b 20-msamples/s low-power cmos adc. *IEEE Journal of Solid-State Circuits*, 30(5):514–521, May 1995.

[22] R. Van De Plassche. *Integrated Analog-to-Digital and Digital-to-Analog Converters*. Kluwer Academic Publishers, 1994.

[23] J. Doernberg, H. S. Lee, and D. A. Hodges. Full-speed testing of a/d converters. *IEEE Journal of Solid-State Circuits*, 19(6):820–827, December 1984.

[24] N. Tan. *Oversampling A/D Converters and Current-Mode Techniques.* PhD thesis, Linkoping University, 1994.

[25] J. C. Candy and G. C. Temes. *Oversampling Delta-Sigma Data Converters.* IEEE Press, 1992.

[26] B. Razavi. *Design of Analog CMOS Integrated Circuits.* McGraw-Hill, 2001.

[27] B. Wooley. Ee 315 vlsi data conversion circuits. Lecture Notes.