Design Exploration of a 65 nm Sub-V_T CMOS Digital Decimation Filter

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***Abstract*—This paper presents an analysis on energy dissipation of digital half-band filters operating in the the sub-threshold (sub-V_T) region with throughput and supply voltage constraints. A 12-bit filter is implemented along with various unfolded structures, used to form a decimation filter chain. The designs are synthesized in a 65 nm low-leakage CMOS technology with various threshold voltages. A sub-V_T energy model is applied to characterize the designs in the sub-V_T domain. The results show that the low-leakage standard-threshold technology is suitable for the required throughput range between 250 Ksamples/s and 2 Msamples/s, at a supply voltage of 260 mV. The total energy dissipation of the filter is about 205 fJ per sample.**

I. Introduction

Miniaturized wireless devices are gaining importance in medicine, sensor networks, and many other applications. Engineers aim to develop ultra compact and low energy implementations that may be used in devices like hearing aids, medical implants, and remote sensors. In such devices minimal energy dissipation in active and standby mode, is of highest importance as it makes the battery last longer.

The conducted project targets an ultra low-power wireless receiver. The design constraints are below 1 mW and 1 μW power consumption in active and standby mode, respectively. The device has to handle data rates up to 250 kbits/s, and realization on a single chip with an area of 1 mm^2 in 65 nm CMOS. A block diagram shows the receiver system in Fig. 1, containing a RF front-end (2.5 GHz), an analog-to-digital converter, a digital baseband for demodulation and control, and finally, a decoder that processes the received data packets.

The main focus of this paper is on the digital baseband part of the receiver system. The first task of the digital baseband implementation is to decimate data from 4 Msamples/s of the $\Delta\Sigma$ ADC to 250 Ksamples/s. Therefore, a chain of four decimation filters, that each decimates by a factor of two, needs to be applied. To achieve ultra-low energy dissipation, the filters are operated in the sub-threshold (sub-V_T) domain [1]. Consequently, there is a need to optimize the implementation in terms of energy dissipation, area, and throughput for sub-V_T operation.

In Sec. II the applied sub-V_T energy model is briefly presented. In Sec. III an architecture of a Half Band Digital (HBD) filter, implemented as direct mapped as well as various unfolded structures, is presented. In Sec. IV the results attained from the HBD filters are shown and discussed, and finally, the conclusions are drawn in Sec. V.

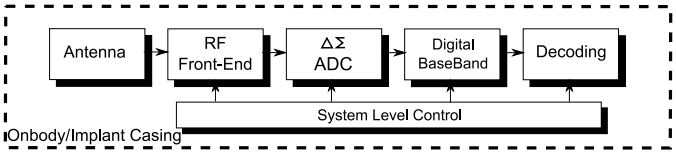

Fig. 1. Receiver system.

II. Sub-V_T Energy Model

The current of a MOS transistor is not equal to zero when the gate to source voltage V_{GS} is equal to or below the threshold voltage V_T, $V_{GS} \leq V_T$, which is an indication for leakage currents, commonly referred to as the sub-V_T or weak inversion conduction [2]. The existent current is due to leakage and is low in amperage. This current is used as the operating switching current in sub-V_T domain. The drawback of sub-V_T implementations is speed penalty, however, ultra low energy requirements are achieved, since order of magnitudes less energy is dissipated compared to super-threshold implementations [2]. The total energy dissipation of static CMOS digital implementations, typically modelled as

$$E_{total} = \underbrace{\alpha C_{tot} {V_{DD}}^2}_{E_{dyn}} + \underbrace{I_{leak} V_{DD} T_{clk}}_{E_{leak}} + \underbrace{I_{peak} t_{sc} V_{DD}}_{E_{sc}}, \quad (1)$$

where E_{dyn} is the average switching energy and E_{leak} is leakage energy dissipated during a clock cycle T_{clk}. The energy dissipation due to short circuit *(E_{sc})* is minor compared to the overall energy dissipation, which therefore is neglected [1]. In (1), E_{dyn} during one clock period is proportional to the switching activity factor *(α)*, and the total switched capacitance of the circuit *(C_{tot})*.

The model used to calculate energy dissipation, delivers SPICE-accurate results [3]. This model calculates total energy dissipation under the assumption that the design is operated on maximum clock frequency is specified as (2), and the key parameters required are obtained during synthesis and high level simulations.

$$E_T = C_{inv} V_{DD}^2 \left[\mu_e k_{cap} + k_{crit} k_{leak} e^{-V_{DD}/(nU_t)} \right], \quad (2)$$

where k_{leak} is average leakage scaling factor of the implementation, normalized to the average leakage current of a single inverter. The scaling factor k_{cap} is the normalized total capacitance of the implementation in terms of a single inverter capacitance. The k_{crit} is a coefficient that measures the critical path delay of the implementation normalized to the delay of a

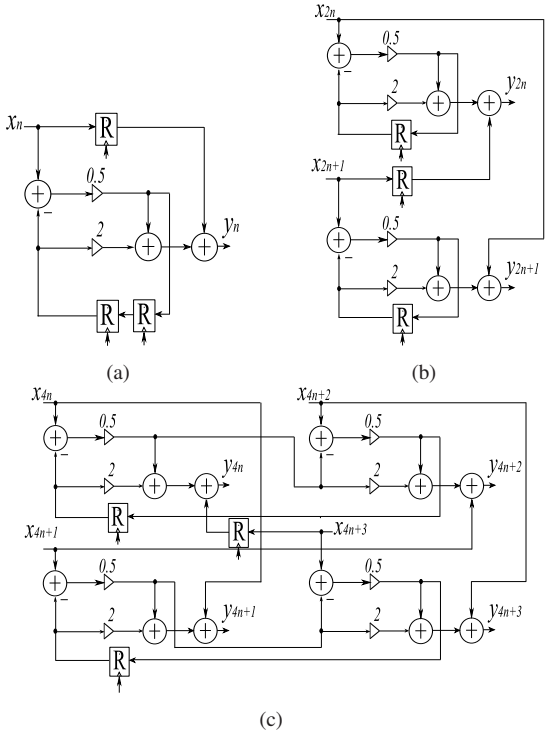

Fig. 2. Half Band Digital Filter. (a) original HBD filter (b) UF2 HBD filter (a) UF4 HBD filter.

single inverter. The average switching activity of circuit per *N* samples operations is μ_e. A process dependent constant called slope factor is *n*, and U_t is the thermal voltage, defined as 26 mV at 300 K. For more details the reader is referred to [3]. When the design is constrained by speed. i.e. the design has to work below the speed that is achievable at the used supply voltage, then the energy dissipation by the design is specified as

$$E_T = \mu_e k_{cap} V_{DD}^2 + k_{leak} I_0 V_{DD} T_{Clk}, \tag{3}$$

where T_{Clk} is the clock time period, and I_0 is the average leakage current of a single inverter when gate to source voltage is equal to zero [1].

III. Filter Architectures

Minimum energy dissipation with medium to high throughput requirement puts stringent constraints on a design. This section presents the HBD filter and the architectural differences in the original and unfolded versions.

A. Half Band Digital Filter

The filter structure for the original implementation, see Fig. 2(a), is a third-order bi-reciprocal lattice wave digital filter, [4]. A HBD filter is considered highly suitable as decimator or interpolator, for sample rate conversions with a factor of two. The benefit of using this type of filter is that all filtering may be performed at lower sample rates, with low arithmetic complexity, therefore, a suitable candidate for both low energy dissipation, and a low chip area requirements [5]. The transfer function of the proposed filter is

$$H_z = \frac{1 + 2z^{-1} + 2z^{-2} + z^{-3}}{2 + z^{-2}}, \tag{4}$$

TABLE I
Extracted Parameter for the Synthesized Implementations

Arch.	Cells	$\mathbf{k}_{leak}$	$\mathbf{k}_{cap}$	$\mathbf{k}_{crit}$	μ_e	Area	$\mathbf{t}_p$[ns]
ORG	Hvt	1113	835	127	0.727	1124	2.84
	Svt	1181	803	112	0.723	1163	1.82
	Lvt	1619	875	101	0.671	1208	1.45
UF2	Hvt	1695	1375	127	0.708	1836	2.84
	Svt	1971	1553	116	0.620	1871	1.89
	Lvt	4485	1434	105	0.720	2069	1.51
UF4	Hvt	3172	2798	164	0.703	3275	3.66
	Svt	3199	2709	150	0.710	3390	2.44
	Lvt	8524	2721	133	0.760	3750	1.90

having the advantage that the filter coefficients are implemented by simple shifts, thereby saving the area, and energy dissipation of the implementation. An initial analysis indicates that the required throughputs would not be achieved by the original architecture if operated in sub-V_T, referred to as (ORG), and therefore, unfolding is applied. Unfolding is a transformation technique that calculate (j) samples per clock cycle, where j is the unfolding factor. Unfolding has a property of preserving the number of delays in a Data Flow Graph (DFG) [6]. The ORG filter architecture is unfolded, by factors of 2 (UF2), and 4 (UF4), see Fig 2(b) and Fig 2(c), respectively. In all unfolded architectures the number of registers remain unchanged, whereas the number of adders scale with the unfolding factor. Furthermore, the critical path in the UF2 remains unchanged to the ORG implementation. However, the critical path for UF4 has increased, since two of the feedback paths does not contain a register. However, more samples are processed per clock cycle, which wins with respect to throughput over a limited increase in the critical path [7].

B. Hardware Mapping

Each architecture was synthesized with Low Leakage (LL) libraries with different threshold voltage options. The first synthesis is performed using high-threshold (Hvt) cells, second, using standard-threshold (Svt) cells and last, using low-threshold (Lvt) cells. Tight synthesis constraints were set to achieve minimum area, minimum leakage, and a short critical path. The parameters for the energy model are retrieved by gate-level simulations with back annotated toggle and timing information, which includes glitches.

IV. Simulation Result

In this section the filter architectures are evaluated with respect to energy, throughput, and supply voltage constraints. The parameters required for the energy model [3] are presented in Table I. The values for k_{leak} follow the area cost, indicating proportional leakage with respect to area for both LL-Hvt and LL-Svt implementations. However, k_{leak} values are higher for LL-Lvt cells. Instead, the critical path (t_p) for LL-Lvt is less than both LL-Hvt and LL-Svt implementations, as expected.

Energy dissipation is calculated under the assumption that the designs operate at critical path speed. Minimizing the energy per clock cycle with respect to supply voltage gives the so called Energy Minimum Voltage (EMV) point [8]. The

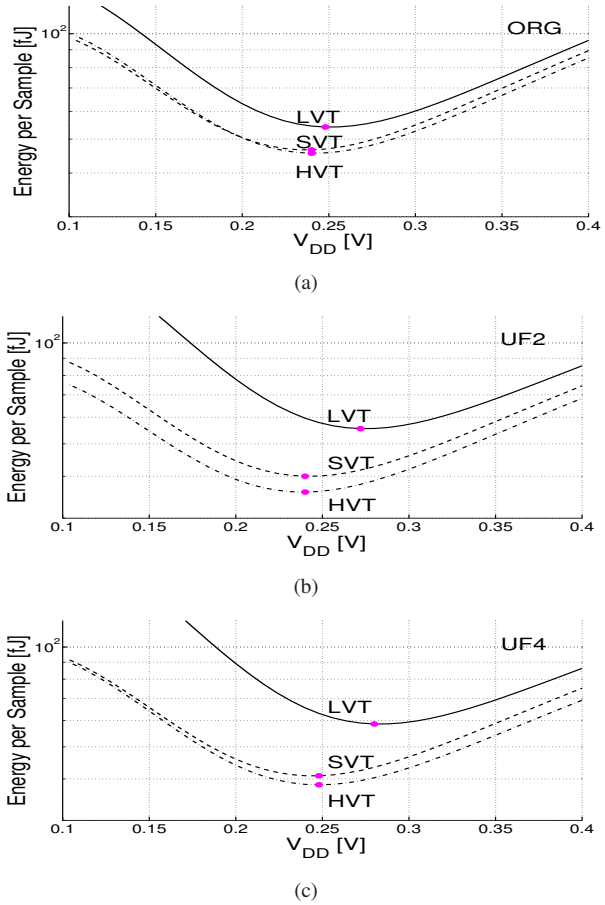

Fig. 3. Energy vs V_{DD} per sample simulation plots of HBD filter architectures, (a) ORG, (b) UF2, (c) UF4.

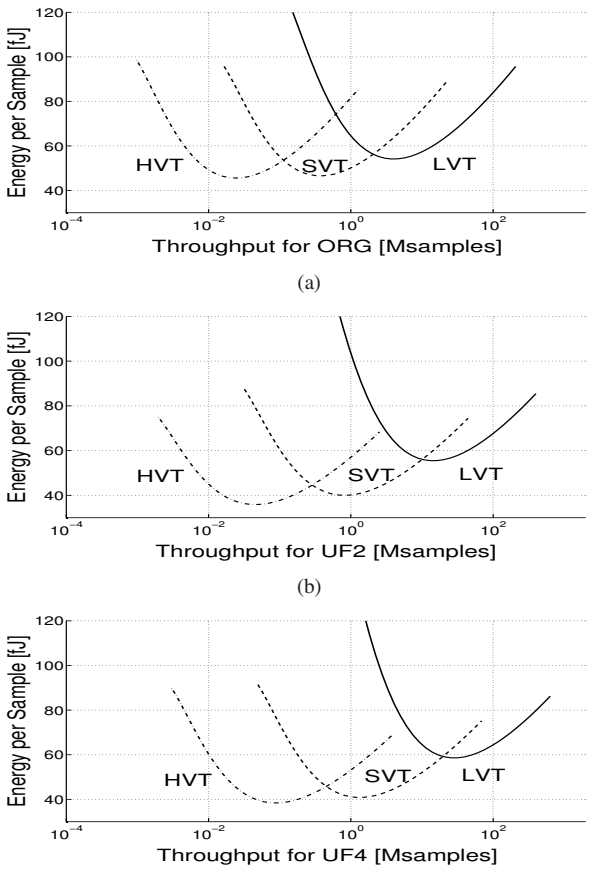

Fig. 4. Energy vs Throughput plots of HBD filter architectures, (a) ORG, (b) UF2, (c) UF4.

designs' energy characteristics, over a scaled supply voltage V_{DD} per sample are presented in Fig. 3. Fig. 3(a), shows the energy dissipated by gate-level implementations of ORG for the various threshold voltage option, indicated as Lvt, Svt, and Hvt. Similarly, Fig. 3(b) and Fig. 3(c), show the energy dissipation curves for the UF2 and UF4 architectures. The dots on the curves indicates EMV for each architecture and threshold voltage type. In all of the cases the minimum energy is achieved by LL-Hvt implementations and UF2 appears to be the architecture that dissipates least energy per sample.

Table II, presents the EMVs of each gate-level implementation, the maximum clock frequency at EMV, the corresponding throughput in samples per second, and the energy dissipated per sample. The UF2 architectures dissipates least energy per sample at EMV. The simulations show that the LL-Lvt implementation is able to operate at much higher frequency at EMV compared to their counterparts. The reason for this behavior is higher currents in the cells, both drive currents and leakage currents. Increased leakage, and drive current, pushes frequency higher to reduce the energy per cycle. Similarly, the LL-Svt and LL-Hvt implementations have frequencies corresponding to their cell currents. The simulations show that the maximum clock frequency increases exponentially with increasing supply voltage i.e., the current increases exponentially in the cells, which leads to a further analysis on energy dissipation versus throughput.

TABLE II
CHARACTERIZATION OF THE IMPLEMENTATIONS AT EMV

Arch.	**Cells**	**EMV** [mV]	**Freq.** [kHz]	**Throughput** [ksamples/s]	**E/smp** [fJ]
ORG	Hvt	241	23	23	45
	Svt	237	398	398	46
	Lvt	251	3710	3710	54
UF2	Hvt	238	23	46	**35**
	Svt	242	383	767	**40**
	Lvt	271	6600	13000	**55**
UF4	Hvt	247	22	88	38
	Svt	241	297	1180	41
	Lvt	280	6500	26	59

A. Throughput Constraints

Fig. 4(c), shows the energy vs throughput plot of UF4 and is shown that UF4-Svt implementation is the most suitable choice of implementation for a throughput requirement within the range of 2 to 20 Msamples/s. Fig. 4(b) and 4(a), show the energy dissipation vs throughput curves for the UF2 and ORG architectures. The LL-Svt implementation of the UF2 architecture is suitable for the throughput range of 250 Ksamples/s to 2 Msamples/s. The throughput constraint for the system in Sec. I are of 2 and 1 Msamples/s for the first two

TABLE III
PERFORMANCES AT REQUIRED THROUGHPUTS

Throughput	**Arch.**	**Vdd** [mV]	**E/smp** [fJ]	**E/smp@260 mV** [fJ]
2 Msamples/s	**UF4**	**260**	**41.6**	**41.6**
	UF2	280	42.7	-
	ORG	300	55.8	-
1 Msamples/s	UF4	240	40.8	52.3
	UF2	**250**	**40.3**	**44.4**
	ORG	280	50.6	-
500 Ksamples/s	UF4	200	45.8	72.2
	UF2	**220**	**40.7**	56.6
	ORG	240	46.8	**52.5**
250 Ksamples/s	UF4	170	53.4	112
	UF2	**200**	**46.4**	81.1
	ORG	220	47.1	**66.3**

decimation filters and for the last two 500 and 250 Ksamples/s. These requirements are fulfilled with least energy dissipation by different architectures using Svt cells. Therefore, further analysis is based on LL-Svt implementations only. Table III, presents the energy dissipation per sample for the required throughputs at corresponding supply voltages for different architectures for LL-Svt implementations. The first filter with a throughput requirement of 2 Msamples/s is fulfilled by an UF4 filter architecture as the most suitable option. Whereas, the second, third and forth filters with throughput requirements of 1 Msamples/s, 500 and 250 Ksamples/s are best achieved by the UF2 filter architecture, the optimal values are shown in bold Table III.

B. Supply Voltage and Throughput Constraints

In [9], is found that the supply voltage value which realizes operation with less than 0.001 failure rate for a 65 nm LL-HVT process is 250 mV and this value is taken as the minimum reliable operating voltage (ROV). The simulations show that the required throughput for the first, and second decimation filter are fulfilled using UF4 and UF2 at 260 mV, and 250 mV, respectively. Having multiple power domains increases cost with respect to area, and energy dissipation, therefore, is not desired. A single supply voltage of 260 mV is introduced as another constraint on the system. The selection of this voltage is based on the analysis that the first filter with a higher throughput constraint is fulfilled by using UF4 at 260 mV. Therefore, 260 mV is selected as a supply voltage constraint and all the filter will operate at 260 mV. The assumption that the data is provided to the filter at critical path speed is not valid anymore. Therefore, the equation (3) for clock constrained systems is used to find the energy dissipation [9]. The last column in Table III, shows energy dissipation per sample at 260 mV, for the three architectures at the required throughputs. Using a single power domain will have an impact on the criteria of selection of the suitable filter structures that are least energy dissipating.

The energy dissipation of the first filter remains unchanged, as UF4 is operated at critical path speed. The energy dissipation of second filter increases, as the implementation is clocked slower than the critical path delay and therefore, there is an increase in leakage energy. However, UF2 is still the most suitable filter architecture at these throughput and supply voltage constraints. The most suitable architecture for throughput requirements of both 500 and 250 Ksamples/s is ORG, shown in Table III. The ORG filter has the least area, therefore, once the implementations are not operating with critical path speed, has an advantage of dissipating less energy because of lesser leakage currents. Hence, with all the requirements in place, all filters in the chain will have LL-Svt implementations, with the first filter being unfolded by 4, the second unfolded by 2, and the last two filters will be the original filter architecture, as shown in Fig. 5. The total energy dissipation per output sample for the filter chain is around 205 fJ.

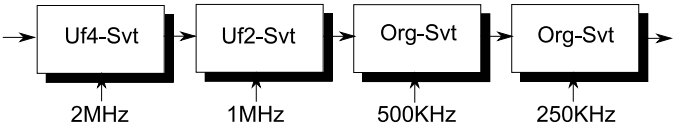

Fig. 5. Suitable Filter Chain for Digital Baseband.

V. CONCLUSION

In this paper various HBD filter structures are evaluated for minimum energy dissipation in the sub-V_T domain for a throughput and voltage constrained system. Different unfolding factors are used to achieve different performances. All filter structures are implemented and simulated using 65 nm LL-Hvt, LL-Svt and LL-Lvt standard cells. The simulations results show that for the required throughput constraints, and using single power domain, the most suitable decimation filter chain dissipates around 205 fJ per output sample. The analysis using a sub-V_T energy model leads to the conclusion that different architectures are suitable for different constraints, and it is vital to find the appropriate architecture that fulfills all the requirements with the least energy dissipation.

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