A 1.8V 12-bit 230-MS/s Pipeline ADC in 0.18µm CMOS Technology

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***Abstract*—This paper describes the implementation of a 12-bit 230 MS/s pipelined ADC using a conventional 1.8V, 0.18µm digital CMOS process. Two-stage folded cascode OTA topology is used for improved settling performance. Extreme low-skew (less than 3ps peak-to-peak) chip-level clock distribution is ensured by five-level balanced clock tree, implemented in low swing current-mode logic. The ADC block achieves a peak SFDR of 71.3 dB and 9.26 ENOB at 230 MS/s, with an input signal swing of 1.5Vpp. The measured peak SFDR at 200 MS/s is 78 dB, while the peak SNDR at 200 MS/s is 59.5 dB. The SFDR and SNDR performance exhibits very flat characteristics, maintaining higher than 53 dB SNDR at 230 MS/s and higher than 58 dB SNDR at 200 MS/s, from DC through Nyquist rate input frequencies.**

I. Introduction

High-performance analog-to-digital converter (ADC) blocks are needed for a very wide range of applications in wireless telecommunications, instrumentation, medical imaging, audio and video processing. Sampling rates in excess of 200 MHz and bit resolution of more than 10 bits are increasingly required to accommodate the very high bandwidth demands in wireless applications [1]-[6]. In addition, the increasing trends towards using deep-submicron CMOS technologies and system-level integration create the need to develop compact, high-performance ADC macros that can be realized with mainstream digital CMOS processes and integrated as building blocks in SoC designs.

The emerging requirements of several high-performance applications also create the demand for sampling rates much higher than a few hundred MHz (typically in the order of 800 MHz to 1 GHz) and a bit resolution of higher than 10 bits, which can only be satisfied by the use of time-interleaved multi-channel ADC architectures [7]. One possible realization of such multi-channel ADCs may rely on a stand-alone front-end S/H (or T/H) unit that is capable of sampling the incoming analog signal at a very high rate, and distribute to parallel ADC channels. In this case, robust performance of the individual channel ADCs and the possibility of background calibration between channels will determine the overall ADC performance.

This paper presents the design, implementation, and the experimental characterization of a 12-bit pipelined ADC block realized using a conventional 0.18um digital CMOS technology, which can be utilized as the key building block of a time-interleaved multi-channel ADC with very high performance, or alternatively, as a stand-alone ADC unit that can be realized in conjunction with other digital functions on chip.

Previously demonstrated examples of Nyquist-rate ADCs with high bit precision using 0.18um CMOS technology and 1.8V supply voltage have been shown to operate at sampling rates of up to 210 MHz [1]. To our knowledge, the present work is the first demonstration of a 12-bit pipelined ADC with 9.26 ENOB in this technology, capable of operating at 230 Ms/s, and with an input swing of 1.5V at 1.8V supply voltage.

The overall converter architecture is presented in Section II, which is followed by the detailed discussion of the circuit implementation in Section III. The measurement results are presented in Section IV, and concluding remarks are provided in Section V.

II. Converter Architecture

The ADC pipeline is composed of a 2.5-bit stage followed by nine 1.5-bit stages and a 3-bit flash converter, as shown in Fig. 1. The sampling capacitor sizes are scaled down twice along the pipeline by a factor of 2, and then remain constant in stages 3 to 10. Two extra stages are added to reduce the quantization noise and the round-off errors in the digital calibration.

For low power consumption, the first stage should resolve the number of bits necessary to reduce the noise constraint of the following stages to a level that can be satisfied with minimum size sampling capacitors. However, in our design, the stage resolution is limited to 2.5bit/stage by the bandwidth limitation of the technology, layout complexity, and the requirement for low input capacitance. With less than 2ns available for settling, the parasitic capacitances of the large transistors are comparable to the sampling capacitance. This

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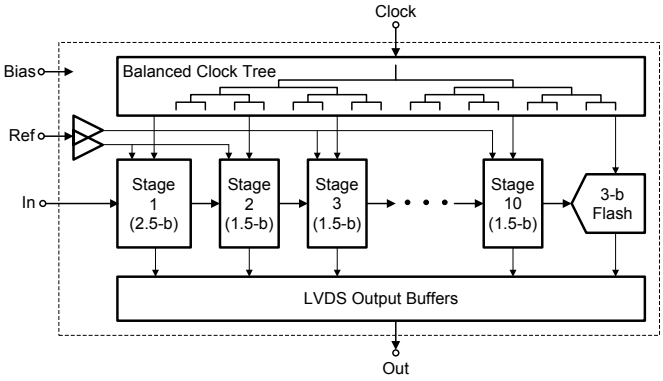

Figure 1. Pipelined ADC architecture

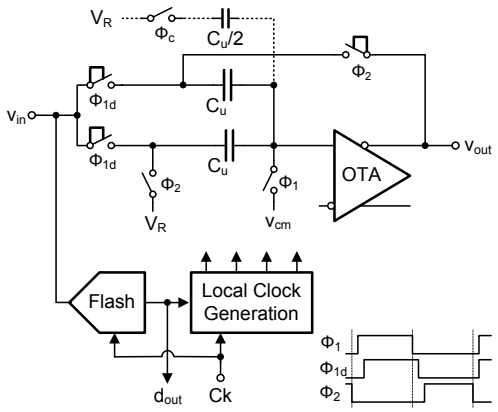

Figure 2. Simplified half-circuit diagram of a 1.5-bit pipeline stage

presents a critical trade-off: when the amplifiers become self-loaded, the power efficiency of the pipeline drops. As the number of bits in the stage grows, the routing of the switch control signals becomes more complex. Because margins for timing constraints (non-overlap) must be small in order to maximize available settling time, it becomes difficult to distribute the signals within the stage with low enough skew.

Separate buffers are used for the reference voltages of the first two stages and the remaining stages to avoid cross-talk through the reference lines. Because even and odd stages work in opposite phase, the first two stages never use the references at the same time. Offset errors between the references for the two parts are corrected by the digital calibration.

A low-skew clock tree distributes the clock to all stages. Using a very robust, low-skew clock distribution scheme represents one of the key design decisions of this ADC architecture. If the clock rippled along the pipeline from back to front to ensure that inter-stage timing constraints are met, the available amplifier settling time would be reduced, and later stages would be switching at the sampling instant of earlier, more sensitive, stages.

All digital post-processing is done off-chip in the current prototype. Having access to all digital information helps debugging the circuit and makes the ADC more useful as a data source for testing alternative calibration algorithms.

III. Circuit Implementation

A. Pipeline Stages

Figure 2 shows a simplified half-circuit diagram of a 1.5-bit pipeline stage. An extra capacitor of half the unit capacitor size has been added to the multiplying-digital-to-analog-converter (MDAC) to implement the digital self-calibration method proposed in [8]. This calibration compensates the effects of capacitor mismatch, finite amplifier DC gain, and reference voltage mismatch between the stages. It works in the foreground, i.e. normal operation of the ADC is interrupted during calibration.

Each stage locally generates the clock phases needed to control the MDAC and the quantizer. The comparators of the quantizer work with current-mode-logic (CML) levels at a nominal differential output swing of $800mV_{pp}$ to reduce switching noise. Local level converters (section III.D) are used to generate the full-swing signals needed to drive the switches.

The sampling switches are bootstrapped in order to reduce and to linearize their on-resistance and to suppress signal dependent charge injection. To improve amplifier settling, the feedback switches are also bootstrapped.

Since the amplifier is used only during half of the clock cycle, and consecutive stages work in opposite phase, a single amplifier could be shared between two successive stages. However, the required additional switches slow down the amplifier settling transient, and increase design complexity [1]. Because in this design we try to push the sampling rate as close as possible to the technology limit, no amplifier sharing is used.

B. OTA Design

Figure 3 shows the OTA topology used in all stages. A folded cascode stage is followed by a common-source stage and cascode compensation is used for good settling performance. The common-mode feedback loop is closed by a switched capacitor network sensing the output common-mode error, and a current mirror inverting the phase of the feedback signal (not shown on schematic).

To simplify the layout effort, the amplifiers in the 1.5-bit stages are all identical scaled versions of the first stage amplifier. Overall power dissipation can be further reduced by using single-stage OTAs in later stages.

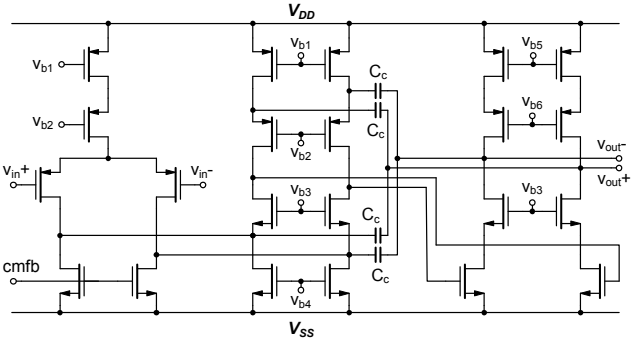

Figure 3. Schematic of the stage amplifier

C. Clock Distribution Network

To implement a low skew clock distribution network with very low noise injection to the substrate and supply, differential CML buffers have been employed. To minimize the skew among the sampling clocks of different stages, the multi-level balanced distribution topology shown in Fig. 4 has

been used. Based on this topology, the required output clock phases are constructed step by step from the main input clock by a tree of buffers. As illustrated in Fig. 4, each buffer stage drives two buffers with a symmetric routing to minimize the skew. To produce clocks for eleven pipeline stages, five levels of buffers are needed, and dummy buffers are placed where necessary to balance the interconnect loading.

According to post-layout Monte Carlo simulations, the total peak-to-peak skew among the channels is less than 3ps, while the total delay can change by 30% over process corners (including the bias current variations).

To design a power efficient clock distribution network, power consumption of the buffers is scaled according to the capacitive loading of each buffer. Figure 5 shows a general view of the proposed clock tree followed by a CML-to-CMOS converter stage. To have a balanced design from settling point of view, it is assumed that the time constant at the output of all buffer stages are equal, i.e.:

$$\tau_i = R_i(C_{P(i)} + 2C_{IN(i+1)}) = \alpha T \qquad (1)$$

where R_i is the load resistance of the CML buffer, T is the clock period, and $\alpha << 1$ is selected in order to have complete settling. The coefficient 2 in front of $C_{IN(i+1)}$ appears because each buffer in the clock tree drives two buffers. Assuming that minimum length (L_{min}) NMOS transistors are used for all buffers, and assuming that $V_{SW(i)} > \sqrt{2}\, V_{DSsat(i+1)}$ (i.e. the current is switched completely by the differential pair), it can be shown that:

$$\tau_i = \frac{V_{SW(i)} \cdot C_{P(i)}}{I_{SS(i)}} + \frac{8L_{\min}^2}{\mu_n} \cdot \frac{I_{SS(i+1)}}{I_{SS(i)}} \cdot \frac{1}{V_{SW(i)}} \qquad (2)$$

where I_{SS} is the tail bias current of CML buffer as shown in Fig. 5 and μ_n is the electron mobility in the NMOS devices. From (2) it can be concluded that higher voltage swing in each stage can reduce the input capacitance of the next stage because of smaller NMOS device sizes of that stage. Therefore, in stages where the load capacitance is dominated by the input capacitance of the next stage, increasing the voltage swing helps to reduce the power consumption while in the stages where the load capacitance is dominated by interconnections (C_P), lower voltage swing is preferred to reduce the power consumption.

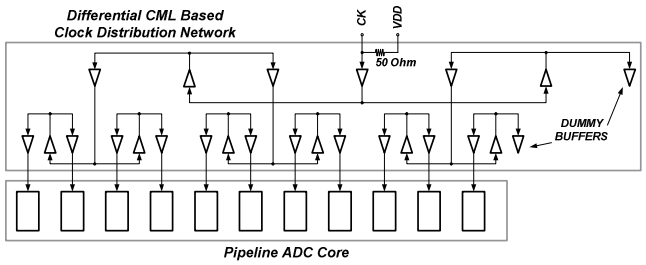

Figure 4. Clock distribution system using differential CML buffers

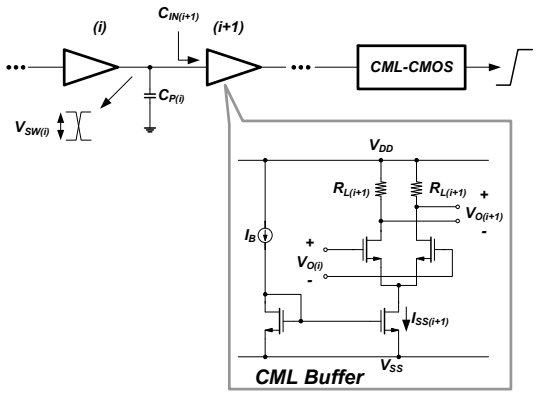

Figure 5. CML buffer chain followed by a CML-to-CMOS converter circuit

D. *CML-to-CMOS level converter*

A CML-to-CMOS level converter (Fig. 6) is used in front of each ADC stage to produce the CMOS level sampling clock. The core of the converter circuit is a fully symmetric amplifier with a differential input. The input differential pair switches the current between one of the output branches where the current is converted to CMOS voltage levels. Clamping circuits are used to limit the voltage swing at the output nodes of the CML-to-CMOS converter and avoid complete switching of the output stage devices. In this way, the speed of operation can be increased and the delay reduced. The positive feedback nature of the clamping circuit also helps to speed up the switching process. Compact layout of this circuit helps to minimize the effect of parasitic capacitances and hence operate in very high speeds. The total delay of this circuit based on post-layout simulations is 200ps when consuming a total of 370µA. The delay can be further reduced by increasing the tail bias current.

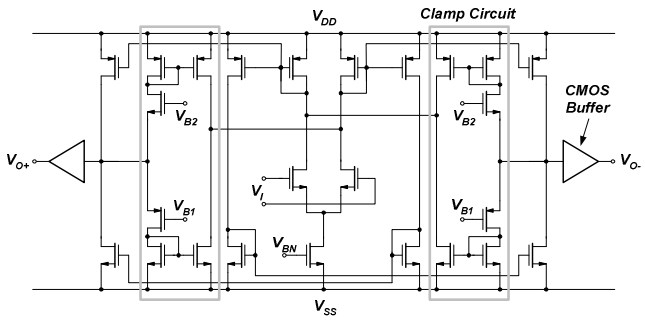

Figure 6. CML-to-CMOS level converter circuit

IV. MEASUREMENT RESULTS

The ADC has been fabricated in a 0.18µm 1-poly 6-metal CMOS technology. Table I summarizes the performance of the ADC after performing digital correction using the parameters obtained by running the ADC in calibration mode.

Figure 7 shows the SNDR and SFDR versus sampling frequency at fin = 20MHz. The dynamic performance versus input frequency at 200MS/s and 230MS/s is shown in Fig. 8. Note that especially the measured SNDR characteristics remain within a very flat band of ±2dB from near-DC through Nyquist rate input frequencies, maintaining better than 8.5 ENOB at 230 MS/s, for all input frequencies.

The effect of calibration on the signal spectrum is illustrated in Fig. 9: after digital correction, the relative power of the largest spur is reduced by about 6dB.

The power dissipation of the analog core is measured as 270mW. Figure 10 shows the chip microphotograph.

TABLE I. SUMMARY OF MEASUREMENT RESULTS

Resolution	12 bit
Sampling Rate	230 MS/s
Technology	0.18-um 1-P 6-M CMOS w/ MiM
Supply Voltage	1.8 V
Full scale input	1.5 V_{pp} (differential)
Analog Core	270 mW
Clock Tree	310 mW
ADC Core Area	1.4 mm^2
Clock Tree Area	0.57 mm^2
SNDR	57.5 dB @ fin = 1 MHz
f_{sample} = 230MS/s	54.4 db @ fin = 114 MHz
SFDR	71.3 dB @ fin = 1 MHz
f_{sample} = 230MS/s	71.2 dB @ fin = 114 MHz

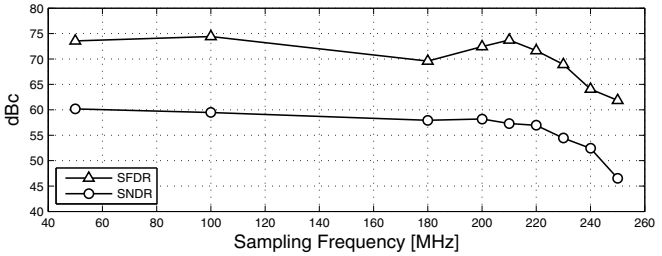

Figure 7. Measured SNDR and SFDR versus sampling frequency at f_{in} = 20MHz

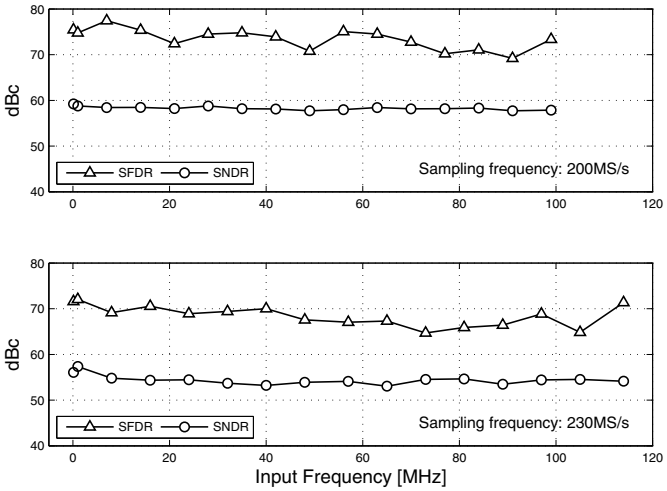

Figure 8. Measured SNDR and SFDR versus input frequency at 200MS/s (top) and at 230MS/s (bottom).

V. CONCLUSIONS

A 12-bit 230MS/s pipelined ADC is demonstrated, using a conventional 1.8V 0.18µm CMOS technology. The ADC achieves a peak SFDR of 71.3dB and 9.26 ENOB at 230MS/s, with an input signal swing of 1.5V. As such, the presented ADC exhibits a very favorable figure-of-merit for this technology node.

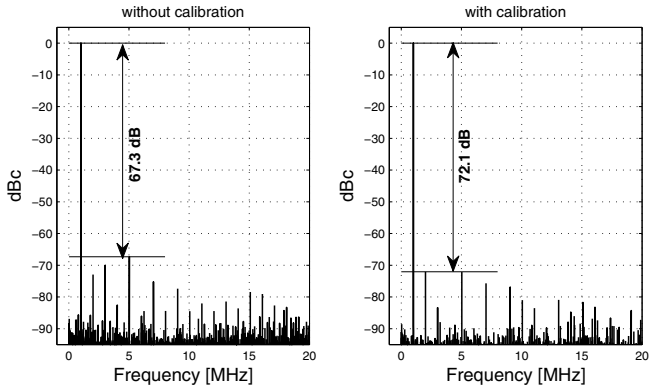

Figure 9. Low frequency section (DC to 20 MHz) of measured signal spectrum at 230 MS/s and f_{in} = 1MHz without calibration (left) and with calibration (right).

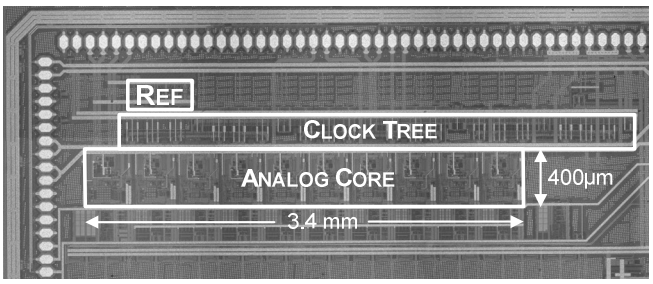

Figure 10. Chip microphotograph showing the analog core, the clock tree and the reference voltage buffers.

REFERENCES

[1] J. Li, R. Leboeuf, M. Courcy, and G. Manganaro, "A 1.8V 10b 210MS/s CMOS Pipelined ADC Featuring 86dB SFDR without Calibration," Proc. IEEE Custom Integrated Circuits Conf. (CICC), pp. 317-320, Sept. 2007.

[2] S.-C. Lee, Y.-D. Jeon, K.-D. Kim, J.-K. Kwon, J. Kim, J.-W. Moon, and W. Lee, "A 10b 205MS/s 1mm2 90nm CMOS Pipeline ADC for Flat-Panel Display Applications," IEEE Solid-State Circ. Conf., Dig. of Technical Papers, pp. 458-615, Feb. 2007.

[3] C.-C. Hsu, C.-C. Huang, Y.-H. Lin, and C.-C. Lee, "A 10b 200MS/s pipelined folding ADC with offset calibration," Proc. of the 33rd European Solid-State Circ. Conf., pp. 151-154, Sept. 2007.

[4] Y. Chen, Q. Huang, and T. Burger, "A 1.2 V 200-MS/s 10-bit Folding and Interpolating ADC in 0.13-µm CMOS," Proc. of the 33rd European Solid-State Circ. Conf., pp. 155-158, Sept. 2006.

[5] Y.-J. Kim, Y.-J. Cho, D.-H. Sa, and S.-H. Lee, "A 10 b 200 MS/s 1.8 mm2 83 mW 0.13 µm CMOS ADC Based on Highly Linear Integrated Capacitors," IEICE Trans. on Electronics, Oct. 2007.

[6] B. Hernes, J. Bjornsen, T. N. Andersen, A. Vinje, H. Korsvoll, F. Telsto, A. Briskemyr, C. Holdo, and O. Moldsvor, "A 92.5mW 205MS/s 10b Pipeline IF ADC Implemented in 1.2V/3.3V 0.13um CMOS," IEEE Solid-State Circ. Conf., Dig. of Technical Papers, pp. 462-615, Feb. 2007.

[7] C.-C. Hsu, F.-C. Huang, C.-Y. Shih, C.-C. Huang, Y.-H. Lin, C.-C. Lee, and B. Razavi, "An 11b 800MS/s Time-Interleaved ADC with Digital Background Calibration," IEEE Solid-State Circ. Conf., Dig. of Technical Papers, pp. 464-615, Feb. 2007.

[8] L. Sumanen, M. Waltari, T. Korhonen, and K. Halonen, "A digital self-calibration method for pipeline A/D converters," Proc. IEEE Symp. On Circ. And Syst. (ISCAS), pp. 792-795, vol. 2, May 2002.