Ömer Can Akgün, PhD

https://ocakgun.com

EXPERTISE

Researcher and educator in the field of bioelectronics and medical devices with broad experience in the design of analogue, digital, and mixed-signal systems. Expert in ultra-low energy, sub-threshold and asynchronous circuit design, characterisation, implementation, and electronic design automation. Industrial and academical experience in RFID protocols, customised RTL-to-GDS and analogue design automation flows, and analogue/digital/mixed-signal design in various process nodes (0.7 um down to 40 nm).

FIELDS OF INTEREST

Implantable self-powered intelligent biomedical systems, brain-circuit interfaces, bioelectronic medicine. Ultra-low energy and asynchronous energy-autonomous circuits and systems. Design automation and characterisation of sub-threshold minimum energy circuits. Artificial intelligence and neuromorphic circuits. Time-mode and asynchronous signal processing.

EDUCATION

Swiss Federal Institute of Technology Lausanne, Switzerland
Ph.D. in Microsystems and Microelectronics January 2005 - November 2009

Dissertation Title: Energy Efficiency Enhancement of Sub-threshold Digital CMOS - Modelling, Technology Selection, and Architectural Exploration.
Advisers: Prof. Yusuf Leblebici and Prof. Joachim Rodrigues.

The Ohio State University Columbus, OH, USA
M.Sc. in Electrical Engineering September 2002 - March 2004

Thesis title: Design Approaches for Low-Power Reconfigurable ADCs.
Adviser: Prof. Mohammed Ismail.

Istanbul Technical University Istanbul, Turkey
B.Sc. in Electronics and Telecommunication Engineering September 1998 - June 2002

Thesis title: Integrated Circuit Implementation of Voltage Controlled LC Tank Oscillators.
Adviser: Prof. Ali Zeki.

WORK-RESEARCH-TEACHING EXPERIENCE

Delft University of Technology - Section Bioelectronics Delft, the Netherlands
Marie Sklodowska-Curie Actions Research Fellow / PD Fellow September 2017 -

- Designed and taped-out ultra-low energy sensors and signal acquisition systems for biosignal sensing and processing in 40 nm, implemented designs offer orders of magnitude lower energy dissipation when compared to the literature (fJ-pJ/per measurement range).
- Implemented automated design, verification, and measurement/characterization flow for time-mode circuits.
- Designed and taped-out various time-mode asynchronous TDCs with digital error correction in a 0.18 μm process for energy efficient time-mode signal processing.
- Designed a 128-sensor, time-mode compressed sensing system. The designed and simulated system reduces the power consumption per channel by up to 95% when compared to the implementations in the literature.
- Implemented an extremely energy efficient asynchronous time-mode digit classification neural network (>89.6% energy reduction).
- As part of the MSCA project, research on time-mode implementation of a remote neural recording, signal processing and communication system. Designed system consumes 11 nW for recording and transmitting EEG signals.
- Implementation and tape-out of two time-mode multi-dimensional package integrity monitoring chips. Manufactured chips qualitatively and quantitatively track the package integrity with high precision and one of the designs has a measurement capability of up to **0.5 peta-ohms**.
- Supervising four master's thesis projects.

MystIC Microelectronics İstanbul, Turkey
Founding Manager April 2011 - August 2017

- *ASIC driver for LED Lighting applications*
  Designed the ASIC LED driver in a high-voltage 0.7um process for the TL 2 million EVATEG project in collaboration with Ozyegin University.
- *EPC Gen 2 RFID Baseband*
  Design and implementation of a near-threshold EPC Gen 2 compatible RFID baseband engine in a 0.18 um process using Synopsys digital design flow for a TL 1 million project for Gate Electronic. Created and realised the digital core from RTL to GDS. Modified the PDK for interoperability between different EDA tools and for top-level implementation in Synopsys ICC.
- *Sub-threshold Digital Circuit Analysis and Optimisation Software*
  Created rapid-analysis and optimisation software for sub-threshold digital circuit design and implementation using Synopsys analogue and digital design flows. The software allows rapid characterisation of digital cores over many process nodes for sub-threshold operation for a continuous range of supply voltages and operating frequencies while taking PVT variations into consideration.
- Obtained a grant based on a business plan for founding an ultra low-energy microelectronics design house from the Ministry of Science, Industry and Technology worth EUR 50,000.

Özyeğin University İstanbul, Turkey
Assistant Professor June 2011 - June 2012

- Prepared and taught undergraduate level EE 202 - Circuit Analysis course. Designed and supervised the labs for the course. Course evaluation scores given by the students ranged from 4.8/5 to 5/5.
- Participated in multiple project proposals both at home and abroad.

Lund University Lund, Sweden
Postdoctoral Research Fellow November 2009 - February 2010

- Implemented a synchronous sub-threshold cardiac event detector with asynchronous power shutdown (65 nm).
- Implemented a self-timed sub-threshold cardiac pacemaker event detector (65 nm).
- Low-energy sub-threshold measurement of previously implemented cardiac event detector chips. Designed a custom PCB for ultra-low current (pA-nA range) measurement, automated the measurements using an FPGA for external control.
- Co-supervised a master student thesis project.

Swiss Federal Institute of Technology Lausanne, Switzerland
Research Assistant January 2005 - April 2009

- Investigated the effects of process variations on the sub-threshold energy dissipation and developed a framework for rapid characterisation of sub-threshold circuits. The framework allows the designer to evaluate the sub-threshold performance and energy dissipation of super-threshold designs.
- Worked on the asynchronous implementation of sub-threshold circuits with current sensing completion detection.
- Investigated architectural energy reduction in the sub-threshold domain.
- *12-bit 230 MS/s ADC Design*
  Designed and taped-out a high-speed, high-accuracy 12-bit 230-MS/s Pipelined ADC (0.18 um) as part of an industrial project. Designed the high accuracy on-chip voltage references, boosted sampling switches and CMOS-to-CML converters.
- *DCVSPG - CMOS Sub-threshold Multipliers*
  Researched sub-threshold operation of logic families for energy efficient operation. Based on the findings of the research, implemented a test chip designed with the DCVSPG and CMOS logic families for comparison (0.18 um). Modified the design kit for interoperability between different EDA tools.

- TA for Hardware Systems Modelling I: Helped students during their lab sessions.
- TA for VLSI Design I-II: Prepared the group design project and supervised a group of students during the design of a streaming video processor.
- TA for EDA Labs: Designed, prepared and graded multiple sections of the course for several years.
- TA for Test of VLSI Systems: Designed and prepared multiple lab sections of the course.
- Supervised a master student thesis project.

Lund University Lund, Sweden
Visiting PhD Student - Researcher May 2009 - June 2009

- Worked on the sub-threshold characterisation and implementation of a digital event detector for cardiac pacemakers (65 nm) using Synopsys Front End tools.

Technical University of Denmark Copenhagen, Denmark
Visiting PhD Student - Researcher October 2008 - March 2009

- Worked on the theoretical aspects of asynchronous operation in the sub-threshold regime.
- Developed a novel asynchronous latch controller for current sensing completion detection. The designed controller was verified using both intensive HSPICE timing simulations for meta-stability and Petrify for correct operation.
- Investigated optimum process selection for sub-threshold digital circuits.

The Ohio State University Columbus, OH, USA
Master of Science in Electrical Engineering September 2002 - March 2004

- *Reconfigurable ADC Implementation*
  Researched and developed a low-power reconfigurable pipelined ADC architecture that scales power linearly with the required conversion speed. The designed and implemented 10-bits 20 MS/s pipelined/cyclic hybrid ADC (0.5 um) was later migrated to a more advanced process node and employed in a GSM/UMTS multi-standard receiver as part of a Semiconductor Research Corporation (SRC) Research Task. Simulations and results analysis were automated using the Skill language and Ocean scripts in Cadence Design Framework.
- *Multi-standard CMOS LC VCO*
  Designed and taped-out a Wide-band, CMOS LC Tank VCO for GSM/UMTS Applications (0.18 um) (SRC-INTEL Funded project). SpectreRF and ADS were used during the design of the VCO. ASITIC and ADS were used for on-chip inductance design and characterisation. The designed VCO satisfied the phase-noise and tuning constraints for multi-standard operation.
- *Geometrically optimised OTAs*
  Designed, taped-out and measured several geometrically optimised OTA topologies (0.5 um). Geometrical optimisation was developed for the lowest power consumption under GBW and area constraints in Matlab and the test chip was implemented in Cadence Analogue Design environment.
- Designed and taped-out a programmable prescaler (0.5 um).

Istanbul Technical University Istanbul, Turkey
BSc. in Electronics and Telecommunication Engineering September 1998 - June 2002

- Researched on-chip implementation of LC tank voltage controlled oscillators.
- Characterised and optimised the inductors using magnetic field solvers and geometric programming. Implemented the designed oscillator in a 0.35 um CMOS technology.

GRANTS

2020 - Delft University of Technology - Erasmus University Medical Center Convergence Programme Postdoctoral Research Fellowship, EUR 65,000.

2019 - Delft University of Technology Section Bioelectronics Postdoctoral Research Fellowship, EUR 65,000.

2018 - Young Investigator Training Program (YITP) - Italy, EUR 3,000.

2017 - European Commission Marie Skodowska-Curie Actions Individual Fellowship, Project ATINARI, EUR 152,000.

2011 - Grant by Turkish Ministry of Science, Industry and Technology to start a microelectronics design and consulting company, EUR 50,000.

2009 - Postdoctoral Fellowship grant by Lund University for postdoctoral studies.

TECHNICAL SKILLS

Analogue / Digital VLSI: Cadence Design Framework, ADS, Synopsys Front End and Back End Tools (DC, PrimeTime, IC Compiler, TetraMax, PowerCompiler), Cadence SOCE.

FPGA: Xilinx ISE and Vivado, Altera/Intel Quartus, Yosys/SymbiFlow.

Simulation: HSpice/RF, vcs-mx, Spectre/RF, ModelSim, ASITIC, Matlab, Mathematica.

Verification: Cadence Assura, Mentor Calibre.

HDLs: Verilog, Verilog-AMS, SystemVerilog, VHDL.

Programming: C, shell scripting, TCL, Python, awk, sed, OCEAN and SKILL.

Measurement: Ultra-low current/energy and analogue/digital/mixed-signal measurement, measurement automation using FPGAs.

SERVICE

Reviewer for: IEEE Transactions on Biomedical Circuits and Systems
IEEE International Symposium on Circuits and Systems (ISCAS) Conference
IEEE Biomedical Circuits and Systems (BioCAS) Conference
IET Circuits, Devices and Systems
IET Electronics Letters
Design Automation Conference
Philosophical Transactions of the Royal Society A

Member: IEEE, CAS, SSCS, EMBS